PUBLICATION NO. 980599

1995
1996
UNIVERSAL TIMER/COUNTERS

RACAL-DANA

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PUBLICATION DATE: DECEMBER 1988

FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltage hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC line (mains) through an autotransformer (such as a Variac or equivalent) ensure that the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adaptor.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument:

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation Section.

2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.

3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If at any time the instrument:

- Fails to operate satisfactorily
- Shows visible damage
- Has been stored under unfavorable conditions
- Has sustained stress

It should not be used until its performance has been checked by qualified personnel.

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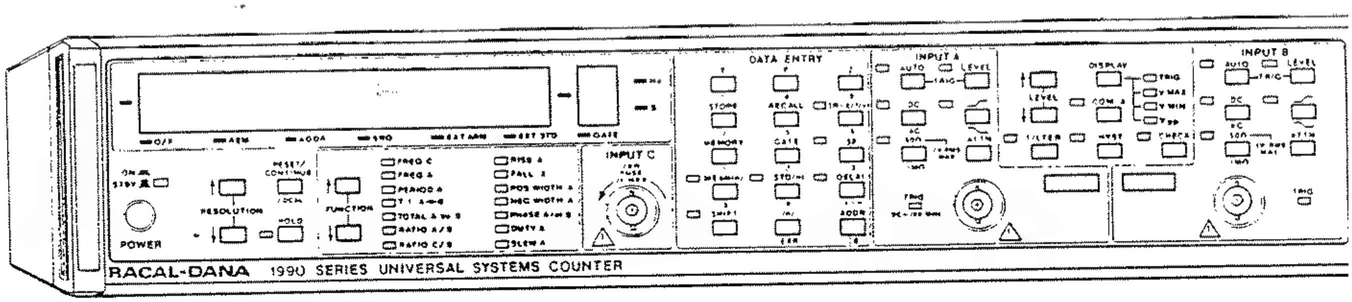


Figure 1.1 - Models 1995/1996 Universal Timer/Counter (1996 Shown)

SECTION 1 GENERAL INFORMATION

1.1 INTRODUCTION

1.1.1 This Instruction Manual provides information for installing, operating, and servicing of Racal-Dana's Universal Systems Counters Models 1995/1996. The designations 1995/1996 are used throughout this manual. Figure 1.1 shows the 1996. Both the 1995/1996 offer universal counter functions using Inputs A and B. The 1996 also provides high-frequency Input C for frequency measurements to 1.3 GHz. Input D, located on the rear panel, provides for external arming and gating. All personnel using the 1995/1996 are encouraged to thoroughly read this manual before operating or servicing either instrument.

1.2 SUMMARY

1.2.1 This manual is organized into eight sections:

SECTION 1. **General Information:** published specifications, safety considerations, product support, general description, and options.

SECTION 2. **Installation & Preparation for Use:** unpacking and initial inspection, reshipment, setup, field installation of options, power connections storage and ventilation.

SECTION 3. **Local Operation:** bench operation, including general operating information, panel descriptions, and measurement procedures.

SECTION 4. **System Operation:** GPIB system operation.

SECTION 5. **Theory of Operation:** general theory of operation.

SECTION 6. **Maintenance:** Performance tests and basic calibration information for the 1995/1996.

SECTION 7. **Drawings:** assembly and schematic drawings.

SECTION 8. **Parts List:** replaceable parts and assemblies.

1.3 SPECIFICATIONS

1.3.1 Table 1.1 lists the 1995/1996 specifications. They specify the performance standards to which either instrument should be tested during necessary calibration and servicing.

Table 1.1 - Technical Specifications

GENERAL DESCRIPTION	
The 1995/1996 system universal counter utilizes a microprocessor-controlled multiple register data acquisition IC for counting and timing to 200 MHz (1.3 GHz on the 1996 with Input C). The counter provides the following measurement functions: frequency, frequency ratio, period, 1-ns resolution time interval, automatic pulse parameters (including duty cycle and slew rate), phase, and totalize. Time interval averaging is available via software-derived functions. The frequency range on Inputs A and B is 0 to 200 MHz; 40 MHz to 1.3 GHz on Input C using an additional board. Trigger levels on Inputs A and B can be set manually via the front panel keypad or via auto-trigger with 50% trigger points. The DC offset component of the input signal may be tracked by auto-triggering in between readings in the manual mode (peak tracking). Use of a timing error correction (TEC) technique permits measurements with 9-digit resolution in one second and a single-shot time-interval resolution to 1 ns. The counter is housed in a 3.5" high X 19" wide full-rack X 19" deep standard corporate enclosure. Total weight does not exceed 22 lbs (10 kg). Unit is adaptable to rack or bench top use.	
INPUT CHARACTERISTICS	
Inputs A and B	
Channel Input:	Start/stop channels for each input provide common measurements for Input A and Input B.
Frequency Range:	
DC Coupled	0 to 200 MHz
AC Coupled	20 Hz to 200 MHz
Sensitivity, Sine Wave:	25 mV rms to 100 MHz 50 mV rms to 200 MHz
Sensitivity, Pulse (Frequency Mode):	150 mV p-p; 2.5 ns min. width with 75 mV overdrive.
Sensitivity, Pulse (T.I. Mode):	75 mV p-p; 5 ns min. width with 35 mV overdrive.
Hysteresis:	Sensitivity reduces by X 4 (nominally). Dynamic range bandwidth limited to approximately 50 MHz.

Table 1.1 - Technical Specifications (Cont'd)

Filter:	Independently selectable Input A and Input B; 100 kHz, nominal. Greater than 20 db attenuation from 10-200 MHz.

Note: The Filter and Hysteresis functions may be combined to increase noise immunity.

Dynamic Range (X1):	75 mV to 10V p-p to 25 MHz 75 mV to 5V p-p to 100 MHz 150 mV to 2.5V p-p to 200 MHz
Signal Operating Range (X1):	-5V DC to +5V DC
Grosstalk at 100 MHz:	500 mV rms*

*Sine wave into either input will not trigger the other input.

Triggering:

Trigger Level Ranges:	5, 50, 250V peak (X1, X10, X50)
Trigger Level:	Adjustable to ±100% of input voltage range with a resolution of 0.2% of input range (10 mV on X1). Level is displayed on front panel.
Trigger Slope:	+ or -, selectable with digital hysteresis compensation.
Trigger Level Setting Accuracy ($25^{o}C \pm 1^{o}C$) (X1 range)	± 1% of trigger level ±10 mV
Trigger Level Temperature Coefficient (X1 range)	± .5 mV/^{o}C

Auto-Trigger

Frequency Range:	DC and 30 Hz to 100 MHz (AC or DC Coupled), usable to 200 MHz
Minimum Amplitude:	150 mV p-p
Accuracy of Trigger Level Readout:	Same as "Read Amplitude Peak" accuracy
Response Time:	650 ms typical 1s maximum

Note: The Auto-Trigger function is independent of the input-signal duty cycle.

Table 1.1 - Technical Specifications (Cont'd)

Coupling:	AC or DC, independently selectable
Impedance:	
High, Separate and Common	1 megohm shunted by 40 pF (nominal)
50 Ohm	50 ohms nominal
Damage Level:	
1 megohm input impedance	X1: 260V (DC + AC rms) DC to 2 kHz
	$5 \times 10^5/f$ V, 2 kHz - 100 kHz
	5V rms, 100 kHz - 200 MHz
	X10,X50:
	260V (DC + AC rms) DC to 20 kHz
	$5 \times 10^6/f$ V, 20 kHz to 100 kHz
	50V rms, 100 kHz to 200 MHz
50 ohm input impedance	5V rms (DC to 200 MHz)
Input C	
Frequency Range:	40 MHz to 1.3 GHz
Sensitivity, Sine Wave:	10 mV rms to 1.0 GHz 100 mV rms to 1.3 GHZ
Dynamic Range:	40 dB to 1 GHz 20 dB to 1.3 GHz
Impedance:	50 ohms nominal, AC-coupled
VSWR	2:1 at 1 GHz
Maximum Operating Input:	1V rms
Maximum Input: (without damage)	7V rms (fuse-protected)
Input D (Gate Control Input)	
Sensitivity, Pulse:	300 mV p-p; 50 ns min. width with 150 mV overdrive

Table 1.1 - Technical Specifications (Cont'd)

Impedance:	10 kilohms shunted by ≤35 pF
Damage Level:	± 20V (DC + AC peak)
Triggering	
Trigger Levels:	TTL or zero-crossing, selectable via specia function or through GPIB interface
Trigger Slope:	+ or -, selectable via special function or GPII
FREQUENCY MEASUREMENT	
Inputs A & B	
Range:	
Input A: (B selectable through Special Function 21 or GPIB)	0 to 200 MHz
LSD Displayed:	(1 ns/Gate Time) X Frequency (i.e., 9 digits in one second)
Resolution:	±(1 X LSD) ± 1.4 X (Trigger Error*/Gat Time) X Frequency
Accuracy:	± Resolution ± Time Base Error x Frequency
Gate Time:	
Range:	Selectable from 200 ns to 100 sec.
Resolution:	≥1 ms, 0.1% <1 ms, 0.1 μs
Input C (1996 only)	
Range:	40 MHz to 1.3 GHz
LSD Displayed:	(1 ns/Gate Time) X Frequency
Resolution:	(LSD)
Accuracy:	± Resolution ± Time Base Error x Frequency

* Refer to Definitions, Trigger Error

Table 1.1 - Technical Specifications (Cont'd)

PERIOD MEASUREMENT	
Range:	5 ns to 1.0 X 10^7 s
LSD Displayed:	(1 ns/Gate Time) X Period
Resolution:	± (1 X LSD) ± 1.4 X (Trigger Error*/Gate Time) X Period
Accuracy:	± Resolution ± Time Base Error x Period
TIME INTERVAL MEASUREMENT	
Input Configuration:	
Separate:	Input A start/Input B stop Input B start/Input A stop (through Special Function 21 or GPIB)
Common:	Input A or Input B start and stop
Range:	-3 ns to 1.0 X 10^7 sec
LSD Displayed:	1 ns (100 ps using Average mode)
Resolution:	± (1 X LSD) ± (Start Trigger Error*) ± (Stop Trigger Error*)
Accuracy:	± (Resolution) ± (Time Base Error) X TI ± (Trigger Level Timing Error**) ± 2ns
Time Interval Delay:	Programmable 200 ns to 100 s
Delay Resolution:	≥1 mSec, 0.1% <1 mSec, 0.1 μs
Delay Accuracy:	Same as Delay Resolution
RISE/FALL TIME	
Range:	5 ns to 25 ms
Minimum Pulse Height:	250 mV p-p
Minimum Pulse Width:	15 ns at signal peaks

* Refer to Definitions, Trigger Error
** Refer to Definitions, Trigger Level Timing Error

Table 1.1 - Technical Specifications (Cont'd)

LSD Displayed:	Same as Time Interval Specification
Resolution:	Same as Time Interval Specification
Accuracy:	Same as Time Interval Specificatio with Trigger Level Timing Error** computed at 10% and 90% trigge points
PULSE WIDTH	
Range:	5 ns to 33 ms (10^7 s for manually se trigger levels)
LSD Displayed:	Same as Time Interval Specification
Resolution:	Same as Time Interval Specification
Accuracy:	Same as Time Interval Specificatio with Trigger Level Timing Error** computed at 50% trigger points
DUTY CYCLE	
Range:	0.01% to 99.99%
Frequency Range:	30 Hz to 100 MHz (to DC for manuall set trigger levels)
LSD Displayed:	0.01% or 1 ns/period x 100% (whicheve is greater)
Resolution:	$\frac{\text{Pulse Width Resolution}}{\text{Period}} \times 100\%$
Accuracy:	$\pm$ LSD $\pm$ $\left(\frac{\text{Pulse Width Accuracy}}{\text{Period}}\right) \times 10$
SLEW RATE	
Range:	10V/s to 2 X 10^9 V/s
Transition Time Range:	5 ns to 30 ms
Minimum Pulse Height:	250 mV p-p

** Refer to Definitions, Trigger Level Timing Error

Table 1.1 - Technical Specifications (Cont'd)

LSD Displayed: $\frac{1\ \text{ns}}{\text{Transition Time}}$ X Slew Rate (to 3 digits)

Resolution: $\pm\left[\frac{\text{(Stop Trig Level-Start Trig Level)} + 10\ \text{mV}}{0.9 \times \text{(Transition Time-Transition Time Resolution)}} - \text{Slew}\right]$

Accuracy: $\pm\left[\frac{\text{(Stop Trig Level-Start Trig Level)} + 20\ \text{mV}}{0.9 \times \text{(Transition Time-Transition Time Accuracy)}} - \text{Slew}\right]$

The magnitude of the slew rate is displayed on the 7-segment display readout. Negative values are obtained on selecting slope \\.

FREQUENCY RATIO MEASUREMENT

Ratio A/B (software)
(Ratio B/A is available via Special Function 21)

Range:

Input A	0 to 200 MHz
Input B	0 to 200 MHz

Accuracy: $\pm$(Accuracy of F_A)/F_A $\pm$(Accuracy of F_B)/F_B

Where F_A and F_B are the frequencies of input signals A and B, respectively.

Ratio A/B (hardware)

Range:

Input A	0 to 100 MHz
Input B	0 to 100 MHz

Table 1.1 - Technical Specifications (Cont'd)

LSD Displayed:	$\dfrac{\text{Ratio}}{F_A \text{ X Gate Time}}$
Where F_A is the higher frequency, connected to the numerator input	
Resolution:	$\pm$ LSD $\pm \dfrac{T_B \text{ X Ratio}}{\text{Gate Time}}$
Where T_B is the denominator trigger error on lower frequency Input B	
Accuracy:	Same as Resolution
Ratio C/B (hardware) (**Ratio C/A** is available via **Special Function** 21)	
Range:	
Input C	40 MHz to 1.3 GHz
Input B	0 to 100 MHz
LSD Displayed:	$\dfrac{\text{Ratio}}{F_C \text{ X Gate Time}}$ X 64
Where F_C is Input C frequency.	
Resolution:	$\pm$ LSD $\pm \dfrac{T_B \text{ X Ratio}}{\text{Gate Time}}$
Where T_B is denominator trigger error on lower frequency Input B	
Accuracy:	Same as Resolution
Ratio C/B (software)	
Range:	
Input C:	40 MHz to 1.3 GHz
Input B:	0 to 200 MHz

Table 1.1 - Technical Specifications (Cont'd)

Accuracy:	$(\pm$ Accuracy of $F_C/F_C) \pm$ (Accuracy of $F_B)/F_B$
Where F_C and F_B are the frequencies of input signals C and B, respectively.	
TOTALIZE A BY B	
(Totalize B by A available via Special Function 21)	
Range:	0 to 100 MHz
Start/Stop:	Input B or manual via Special Function 61
LSD Displayed:	1 Count
Resolution:	LSD
Accuracy:	Same as Resolution
PHASE A RELATIVE TO B	
(Phase B relative to A available via Special Function 21)	
Range:	0 to 360°
Minimum Signal:	150 mV p-p using Auto-Trigger function 25 mV rms Manual Trigger settings
LSD Displayed:	Continuous monitoring of measurement provides optimum resolution based on Period and Time Interval Resolution
Resolution:	$\pm$ LSD $\pm$ $\frac{\text{TI Resolution}}{\text{PERIOD A}} \times 360^\circ$
Accuracy:	$\pm$ LSD $\pm$ $\frac{\text{TI Accuracy}}{\text{PERIOD A}} \times 360^\circ$
GATE TIME	
Range:	200 ns to 100 sec
LSD Displayed:	3 Digit Display

Table 1.1 - Technical Specifications (Cont'd)

TIME BASE (See Option 04E)	
Frequency:	10 MHz
Aging:	<1 ppm per month <2 ppm for first year
Temperature Stability:	± 10 ppm over the range 0° to $50^{\circ}C$, referenced to $25^{\circ}C$
External Standard Input:	
Frequency:	1, 5, 10 MHz
Level:	Min., 500 mV rms, Max., 5V rms
Impedance:	1 kilohm
Internal Standard Output:	
Frequency:	10 MHz
Level:	>1V p-p into 50 ohms
ARMING	
Start Arm:	
Input:	Inputs A, B or D, selectable via Special Functions 82.0-83.3
Start Arm:	(+) or (-) edge, selectable via special function applied to external arm input allows counter to start a measurement cycle

External Gate:	
Input:	Inputs A, B or D, selectable via Special Functions 85.0-88.3
Start Arm:	(+) or (-) edge, selectable via special function applied to external arm input allows counter to start a measurement cycle
Stop Arm:	(+) or (-) edge, selectable via special function applied to external arm input allows counter to stop measurement cycle
Synchronous Window Auto-Trigger: (Syn. Wind. AT)	
Input:	Inputs A, B or D, selectable via Special Functions 91.0-94.3
Start/Stop Edges:	(+) or (-), selectable via special function applied to external arm input allows the auto-trigger function to establish the (+) and (-) signal peaks and trigger level only during the period when the arming signal is present

PEAK SIGNAL MEASUREMENT

The auto-trigger function may be used to determine and indicate the peak maximum, peak minimum, and peak-to-peak values of the measurement signal applied to Inputs A or B.

Display:	Individual 3-digit displays for Inputs A and B.
Frequency Range:	DC and 30 Hz to 25 MHz
Dynamic Range:	.15 to 10V p-p (X1 attenuation)
Resolution:	10 mV (X1 attenuation)
Accuracy:	± 5% of peak-to-peak voltage ± 20 mV for sine waves ± 2% of peak-to-peak voltage ± 20 mV for pulses > 20-ns wide and ≥ 5 ns rise time

Table 1.1 - Technical Specifications (Cont'd)

STATISTICS	
Sample Size:	2 to 9999
Standard Deviation:	Displays Standard Deviation of sample size (n)
Average:	Displays Average (mean) value of sample size (n)
Highest:	Using Special Function 51, the highest value in sample size (n) is displayed
Lowest:	Using Special Function 52, the lowest value in sample size (n) is displayed

MATH

Applies to all counting/timing measurement functions. Note Math Function is applied prior to Statistics Function.

$$\text{Display} = \frac{\text{Reading} - X}{Z} Y$$

Where X, Y and Z are constants entered and stored via the keyboard.

Constant (X, Y or Z) Range:	± 0.000000001E-9 to ± 9999999999 E9
Power-Up Condition:	X = 0 Y = 1 Z = 1

GPIB INTERFACE	
Standard:	IEEE-STD-488-1978
Programmable Controls	All front panel controls with the exception of Power
Universal Commands:	Trigger, Clear, Remote, Local, Local Lockout, Require Service
Data Output Format:	Refer to Tables 4.5 and 4.7
Data Output Rate:	150 readings/second, maximum

Table 1.1 - Technical Specifications (Cont'd)

NON-VOLATILE MEMORY	
Up to 10 complete front-panel settings may be stored for subsequent recall.	
GATE OUT	
A TTL-compatible signal is provided from a rear-panel BNC connector coincident with the measurement gate + 100 nanoseconds.	
TRIGGER LEVEL OUTPUTS	
Start and stop levels are available on the rear panel from BNC connectors for calibration purposes only.	
DISPLAY	
LED: 10 digit display, character size 0.43". Exponent digit, character size 0.43" When measurement exceeds 10 digits, the least significant 10 digits are displayed, and the overflow indicator is lit.	
TEMPERATURE PERFORMANCE	
Operating Temperature:	$0^{\circ}C$ to $+50^{\circ}C$
Storage Temperature:	$-40^{\circ}C$ to $+75^{\circ}C$
POWER REQUIREMENTS:	100, 120, 220, 240V rms ± 10% 50 to 400 Hz ± 10% 80 VA
DIMENSIONS:	88.9 mm (3.5 in) High X 427.0 mm (16.8 in) Wide X 475 mm (18.7 in) deep
WEIGHT:	10 kg (22 lb.)

Table 1.1 - Technical Specifications (Cont'd)

OPTIONS	
Option 01 Rear-Panel Inputs	
Option 04E High-Stability Oven Oscillator	
Proportionally controlled ovenized Internal Frequency Standard	
Frequency:	10 MHz
Aging:	$< 5 \times 10^{-10}$ per day at time of shipment
Temperature Stability:	$< 7 \times 10^{-9}$ over the range $0^{\circ}C$ to $50^{\circ}C$
Line Voltage Stability:	$< 5 \times 10^{-10}$ two minutes after a 10% line voltage change
Option 04R Rubidium Precision Internal Frequency Standard	
Frequency:	10 MHz
Long Term Drift:	$\leq 5 \times 10^{-11}$ per month $\leq 5 \times 10^{-10}$ per year
Temperature Stability:	$\leq 3 \times 10^{-10}$ from $0^{\circ}C$ to $+50^{\circ}C$
Line Voltage Stability:	$\leq 2 \times 10^{-11}$ from ±10% voltage change
Option 60	
Rack mounting kit (fixed)	
Option 65	
Rack mounting kit (slides)	

DEFINITIONS

LSD Least Significant Digit

Trigger Error

$$\text{Trigger error (Seconds)} = \frac{\sqrt{(e_i^2 + e_n^2)}\ \text{(Volts)}}{\text{Input Slew Rate at Trigger Point (V/sec)}}$$

where e_i = input amplifier rms noise, 250 µV rms max

e_n = input signal rms noise in 250 MHz bandwidth

Table 1.1 - Technical Specifications (Cont'd)

Trigger Level Timing Error	
Timing Error = (Seconds)	(Trigger Level Error (V))/ Input Slew Rate at START trig point (V/sec) - (Trigger Level Error (V))/Input Slew Rate at STOP trig point (V/sec)
where Trigger Level Error = ±1% of Trigger Level ±10 mV	

1.4 SAFETY

1.4.1 The 1995/1996 incorporates a protective earth terminal and is designed to meet international safety requirements. Refer to the safety page "FOR YOUR SAFETY" immediately preceding the Table of Contents. Follow all **NOTES**, $\boxed{\text{CAUTIONS}}$, and $\boxed{\text{WARNINGS}}$ to ensure personal safety and prevent damage to the instrument.

1.5 PRODUCT SUPPORT

1.5.1 Racal-Dana supports the 1995/1996 with Product Engineering, Service, and Parts Departments. A complete listing of service centers and field representatives is provided on the last two pages of the manual.

1.6 GENERAL DESCRIPTION

1.6.1 The 1995/1996 is a universal counter designed for system or bench use. Basic measurement functions include Frequency, Period, Time, Ratio, and Totalize. Inputs A and B provide frequency measurement to 200 MHz; Input C (1996 only) extends frequency and ratio measurements to 1.3 GHz. Computational capabilities include Rise/Fall Time, Pulse Width, Phase Measurement, Duty Cycle, Slew Rate, Statistical Data, and Math Operations. Inputs A and B incorporate independent Start and Stop channels with automatic or manual trigger selection. Input D on the rear panel is used for external arming and gating.

1.6.2 Special Functions

1.6.2.1 Both the 1995/1996 provide a set of Special Functions, permitting extended measurements and capabilities beyond the front-panel keyboard. See Subsection 3.4.8 for details.

1.6.3 GPIB Interface

1.6.3.1 The 1995/1996 provides a GPIB interface as standard. This permits the execution of all front-panel operations except power-on and address selection. See Section 4 for GPIB capabilities, addressing, and bus protocol.

1.6.4 Models 1995/1996-02M

1.6.4.1 These two special versions incorporate a MATE(R)/CIIL interface and are available from Racal-Dana.

1.7 OPTIONS

1.7.1 Options available for the 1995/1996 are listed below. Those specified on the original order will be factory installed and ready for use. Section 2 provides information on the field installation of certain options. See the Specifications in Table 1.1 as required.

a. Option 01 - Rear Panel Input
b. Option 04E - High Stability Oven Oscillator
c. Option 60 - Fixed Rack Mount
d. Option 65 - Slide Rack Mount

2.1 INTRODUCTION

2.1.1 This section describes the unpacking and inspection, reshipment, rack installatic miscellaneous option installation, power connections, and storage/temperature requirements f the 1995/1996.

2.2 UNPACKING AND INSPECTION

2.2.1 Before unpacking the counter, check the exterior of the shipping carton for any sig of damage. All irregularities should be noted on the shipping bill. Remove the instrume carefully from its carton, preserving the factory packaging as much as possible. Inspect t counter for any defect or damage. Notify the carrier immediately if any damage is apparei Have a qualified person check the instrument for safety before use.

2.3 RESHIPMENT INSTRUCTIONS

2.3.1 Use the original packaging if it is necessary to return the counter to Racal-Dana 1 calibration and/or servicing. The original shipping carton and the instrument's plastic-fo: form will provide the necessary support for safe reshipment. If the original packaging unavailable, reconstruct it as much as possible. Wrap the counter in plastic; then use plas spray foam to surround and protect the instrument. Reship in either the original or new, stu shipping carton.

2.4 BENCH OPERATION

2.4.1 The 1995/1996 is equipped with a tilt-bail to elevate the front of the instrument easy operation. The tilt-bail is attached to the two front feet on the bottom of the count For use, the bail is pulled down to its vertical position.

2.5 EQUIPMENT RACK INSTALLATION

2.5.1 The 1995/1996 can be mounted in a standard 19-inch equipment rack using either Fixed-Mount Option 60 or Slide-Mount Option 65. Installation instructions for these two opti follow.

2.5.2 Fixed-Mount Option 60 Installation

2.5.2.1 Refer to Figure 2.1 for this procedure. The installation package includes:

a. Flange-Mount angle-brackets (2)

b. Front corner-inserts for nonhandle installations (2)

c. Flathead #8-32 x 1/2 screws (4)

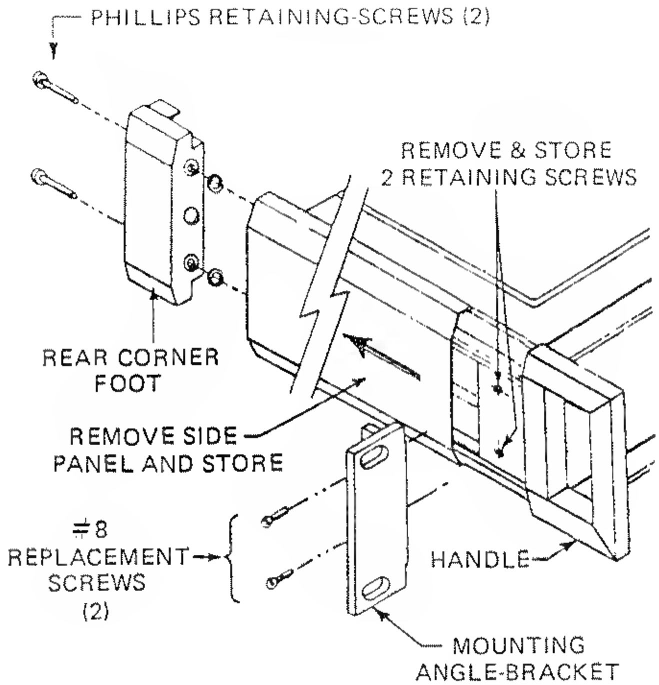


Figure 2.1-Fixed-Mount Angle-Bracket Detail

2.5.2.2 Remove the tilt-bail by applying pressure inward on the bail legs, then unhooking the bail from the bench feet.

2.5.2.3 Remove the bench feet and side panels by completing the following steps:

a. Unscrew the two phillips head screws from each rear corner-foot. This frees the corner-feet, covers, and side panels

b. Remove the two rear corner-feet from the case

c. Place the instrument bottom-up, then slide the bottom cover 1/2 inch towards the rear panel and lift off. The top cover slides off in the same manner

d. Remove the four bench feet from the bottom cover by unscrewing the phillips head retaining screws from each foot

e. Slide the side panels down their retaining tracks towards the rear, then remove the panels. (With side panels off, the retaining screws-2 per side-for the front handles/corner inserts are exposed.)

2.5.2.4 Install the flange-mount angle-brackets by completing the following steps:

a. Remove the retaining screws for both handles/corner inserts, leaving the handles/corner inserts in place

b. Place an angle bracket over each handle/corner insert, aligning the mounti holes over the retaining screw holes

c. Insert two replacement flathead #8-32 x 1/2 screws through each angle brack and handle/corner-insert combination, then screw securely to the case

2.5.2.5 Reassemble the instrument by replacing the top and bottom covers, fitting the frc edge of the covers into the groove in the front panel. Do not attempt to replace t instrument's side panels. Complete the procedure by screwing the two rear corner-feet to t case.

2.5.2.6 Store the following items in a convenient location:

Two side-panels, four bench feet and retaining screws, and four replaced retaini screws from the front handles/corner inserts.

2.5.3 Slide-Mount Option 65 Installation

2.5.3.1 Refer to Figures 2.2-2.6 for this procedure. The installation package includes:

a. Front corner-inserts for nonhandle installations (2) - P/N 454323

b. Flange-Mount angle-brackets (2) - P/N 454422

c. Alignment blocks (6) - P/N 454490

d. Front rack-brackets (2) - Part of P/N 454488

e. Rear rack-brackets (2) - Part of P/N 454488

f. Triple-rail slide-mount assemblies (2) - P/N 454489

g. Self-Anchoring #10-32 tinnerman nuts (12) - P/N 610920

h. Phillips panhead #10-32 x 1/2 screws (8) - P/N 615091

i. Slotted panhead #8-32 x 3/8 screws with nuts, washers, and lock washers each) - Part of 454488

j. Phillips panhead self-tapping #8-32 x 5/16 screws (8) - P/N 610910

k. Phillips flathead #8-32 x 1/2 screws (4) - P/N 615325

l. Phillips panhead #10-32 x 3/4 screws (4) - P/N 615093

m. Alignment #8 x 1/16 (spacers) washers (2) - P/N 610921

n. Cover retaining-brackets (2) - P/N 454597

o. Phillips Flathead Metric Screws M4 x 12 (4) - P/N 611011

2.5.3.2 Prepare the instrument for installing the alignment blocks in the side channels of the unit. Refer to Figures 2.1 and 2.2 and complete the following steps:

a. Remove the two rear corner-feet by extracting the two phillips retaining screws from each foot

b. Slide the top and bottom covers 1/2 inch towards the rear panel, then lift them off

c. Remove the four bench feet and tilt-bail from the bottom cover

d. Slide the side panels down their retaining tracks towards the rear, then remove the panels

e. Store the four panels, four bench feet, and tilt-bail in a convenient location

f. Remove the two front handles/corner inserts from the frame by extracting the two retaining screws from each handle or corner insert

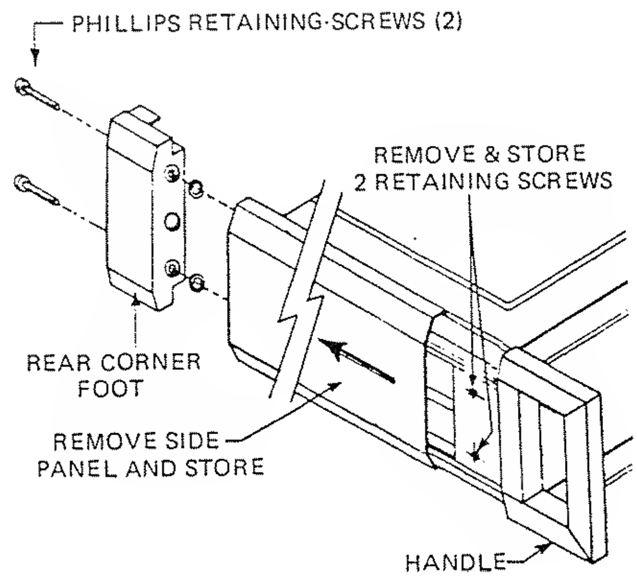


Figure 2.2-Rear Corner Foot, Side Panel, and Handle Detail

2.5.3.3 Refer to Figure 2.3 for alignment block loading. Slide the alignment blocks down the center channel of the frame on each side of the instrument. Three alignment blocks per side should be loaded for full-rack depth units; two blocks for intermediate-rack depth units. The two screw holes in each alignment block should be at center position and below, relative the center channel.

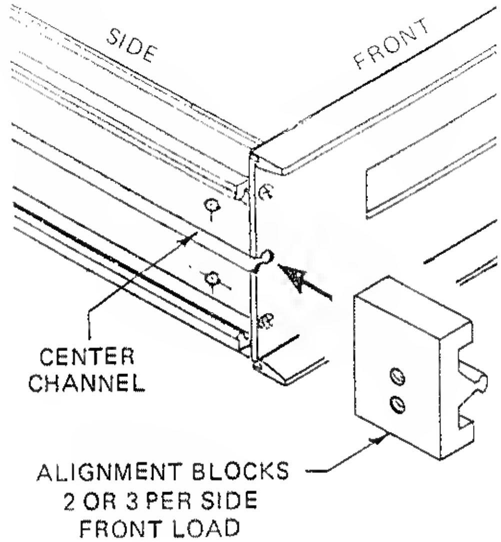


Figure 2.3-Loading the Alignment Blocks

2.5.3.4 Replace the top and bottom covers on the instrument. Fasten the covers using t two cover retaining-brackets (see Figure 2.6) and four phillips panhead screws (two per si originally removed from the rear corner-feet. The instrument is now ready for attachment the two triple-rail slide-mount assemblies.

2.5.3.5 Refer to Figure 2.4A/B. Prepare the triple-rail slide-mount assembly for equipme rack installation. First, note that the instrument-rail and rack-rail holes are accessible eit directly or through the enlarged holes in the center-rail (as the assembly is extended retracted). Complete the following procedure:

a. Place a front rack-bracket (with one mounting slot) on the workbench, slott flange facing down

b. Position the front end (i.e., slide-out end) of the slide-mount assembly over a parallel to the front rack-bracket. The rack-rail should rest within the brack about 3/4 inch from the bracket's front edge

c. Adjust the rails, aligning the front rack-rail hole with the center-rail acc hole and mounting slot in the front rack-bracket. Insert a slotted panhead # 32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to t screw and secure firmly, maintaining the 3/4-inch dimension to the front of bracket

NOTE

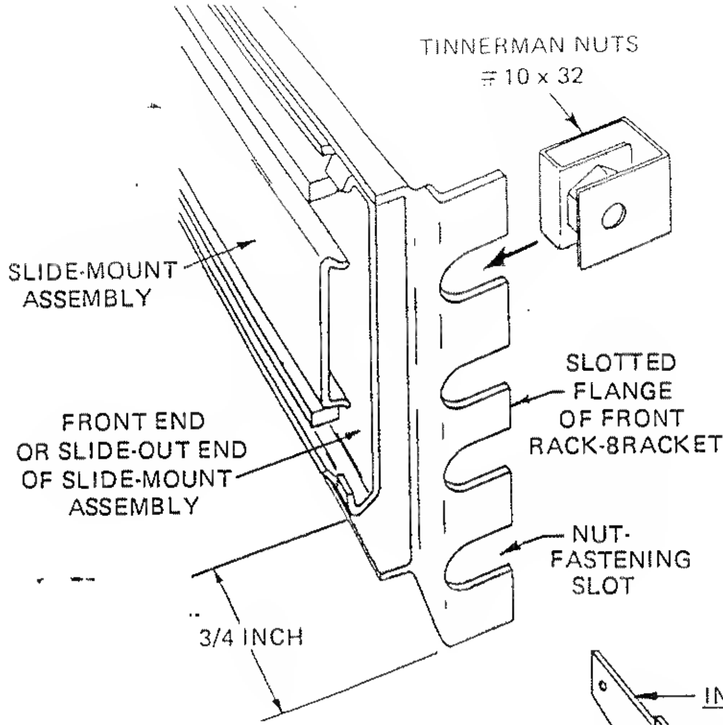
Measure the distance between the front and rear mounting-rails of the rack at this point. If the distance is less than 20 inches, follow instruction "d" next; if the distance is greater than 20 inches, follow instruction "e".

d. Fully extend the slide-mount assembly. Position a rear rack-bracket (with two elongated mounting slots) on the rear of the assembly in the same way as the front rack-bracket. Align the mounting slot closest to the slotted flange with the rear rack-rail nail hole. Insert a slotted panhead #8-32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to the screw and secure the rear rack-bracket loosely to the slide-mount assembly

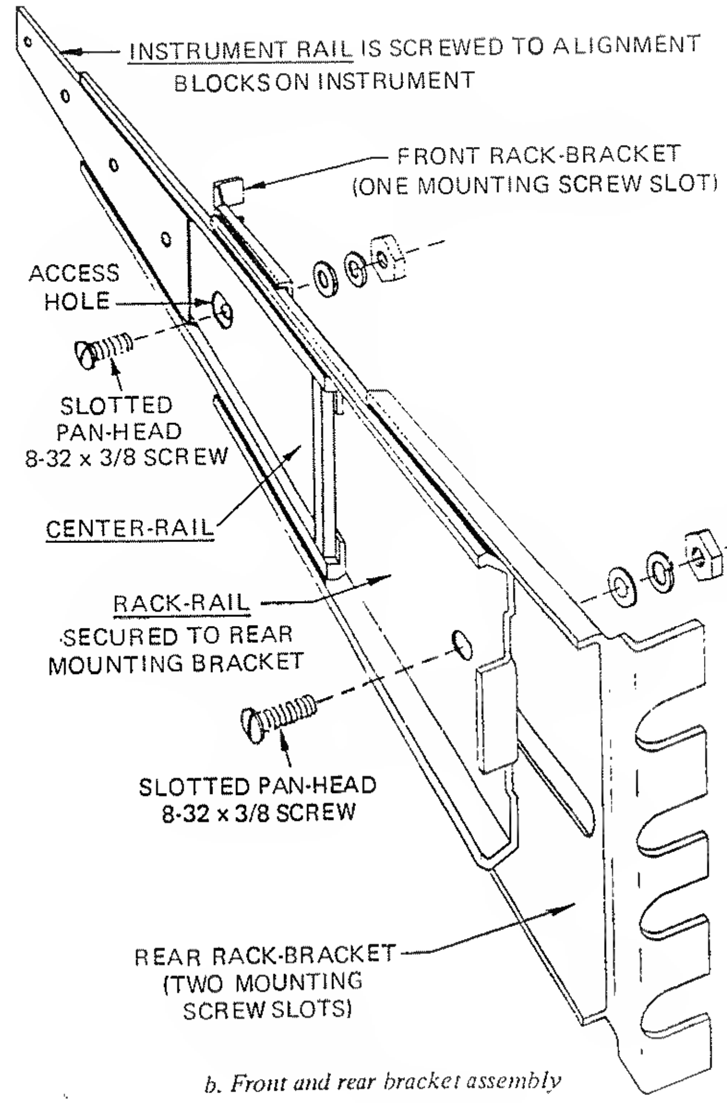
e. Fully extend the slide-mount assembly. Position a rear rack-bracket (with two elongated mounting slots) on the rear of the assembly in the same way as the front rack-bracket. Align the mounting slot farthest from the slotted flange with the rear rack-rail nail hole. Insert a slotted panhead #8-32 x 3/8 screw through the holes. Attach a washer, lock washer, and nut to the screw and secure the rear rack-bracket loosely to the slide-mount assembly

f. Complete the other slide-mount and rack-bracket assembly in the same manner as just described

g. Slide two self-anchoring #10-32 tinnerman nuts on the front and rear rack-brackets at the top and bottom slots of both slide-mount assemblies



a. Front bracket 3/4 inch leading edge



b. Front and rear bracket assembly

Figure 2.4A/B–Slide–Mount and Bracket Assembly

2.5.3.6 The assistance of a second person will be needed for the following instrument-rack assembly. Secure the slide-mount assembly in the designated area of the instrument rack using the procedure below.

NOTE

If the mounting-rail of the instrument rack is tapped for #10-32 screws, drill out two places for each bracket using a 1/4 inch diameter bit. Proceed with the assembly:

a. Hold the front end of the slide-mount assembly behind the front mounting-rail of the rack, while the second person holds the rear end of the assembly

b. Secure the front rack-bracket to the front mounting-rail using two phillips panhead #10-32 x 1/2 screws. Seat the front rack-bracket firmly against the mounting-rail before tightening these screws

c. Install the other front rack-bracket on the front mounting-rail in the same manner

d. Set the front dimension between the two slide-mount assemblies at 16 5/8 inches

e. Adjust the length of the rear rack-brackets to touch the inside of the rear mounting-rail. Tighten the rear rack-bracket assembly screws

f. The distance between the two slide-mount assemblies at the rear-bracket should be 16 5/8 inches. Should a filler plate be required to secure the slide-mount assembly to the rear rack mounting-rail at 16 5/8 inches, use the dimensions given in Figure 2.5 to determine filler-plate size

NOTE

The rear rack-bracket may require adjustment to accommodate the thickness of the filler plate.

g. Secure the rear rack-bracket to the rear rack mounting-rail (or filler plate) using two phillips panhead #10-32 x 1/2 screws in each bracket

h. The triple-rail slide-mount assemblies should move freely to their maximum extended positions. If not, remove any obstacle before installing the instrument

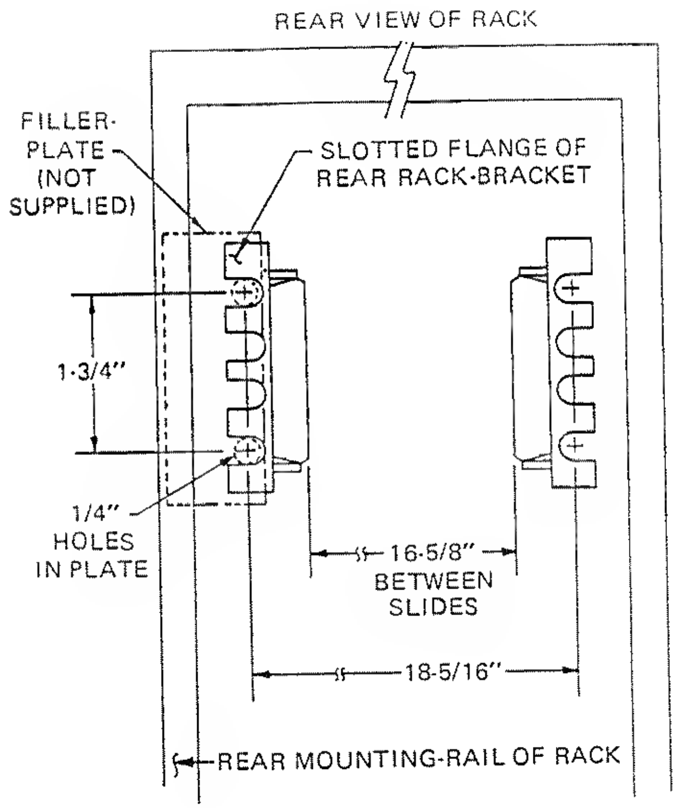


Figure 2.5–Rear End Slide–Mount Rack Dimensions

2.5.3.7 Refer to Figure 2.6 (with inset). The assistance of a second person will be needed for the following slide-mount assembly-to-instrument installation.

a. Extend the rails of the slide-mount assemblies to their maximum position. Insert a phillips panhead self-tapping #8-32 x 5/16 screw inward through the first mounting hole in the instrument-rail. Place an alignment (spacer) washer on the screw on the other side of the instrument-rail

b. Screw the flange-mount angle-bracket to pull-up position on the instrument-rail. Check that the alignment washer remains between the angle bracket and instrument-rail. Repeat this procedure for the other instrument-rail

c. With the help of a second person, position the instrument between the fully extended rails. For full-depth instruments, the rear alignment-block hole should be situated immediately behind the fourth attachment hole in the instrument-rail. For intermediate-depth instruments, the rear alignment-block hole should be located behind the third attachment hole

NOTE

For 3-1/2 inch high instruments, position the rail access hole over the **top** alignment-block hole; for 5-1/4 inch high instruments, use the **bottom** hole.

d. Insert a phillips panhead self-tapping #8-32 x 5/16 screw through the rail access hole and screw it to pull-up position in the alignment block. At the same time, position the flange-mount angle-bracket in its approximate final location in the side frame channels. Align the other alignment-block screw holes with their attachment holes in the instrument-rail. Insert phillips panhead self-tapping #8-32 x 5/16 screws in the alignment blocks and fasten to pull-up position. Repeat this procedure for the other rail

e. Slide the handle/corner insert between the side frames and each angle bracket

f. Align the handle/corner insert and angle-bracket holes with their retaining screw holes in the side frame

g. Insert two phillips flathead #8-32 x 1/2 screws (some models use M4 x 12) through the handle/corner insert and angle-bracket combinations, then fasten firmly to the frame

h. Securely fasten all self-tapping screws in the instrument-rail. The instrument should slide freely on the rails

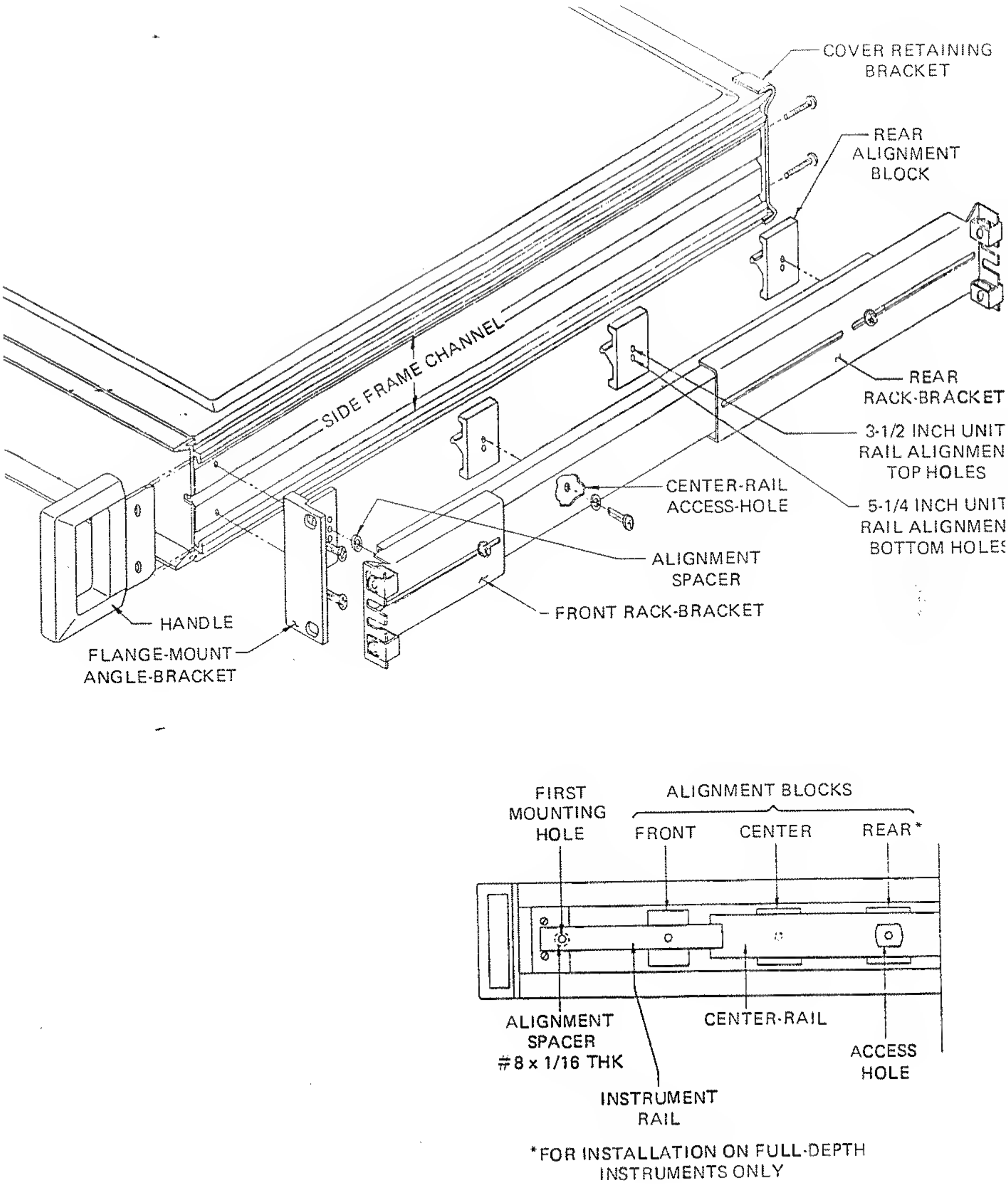


Figure 2.6-Slide-Mount and Instrument Assembly (with inset)

2.5.3.8 The following assembly is required to lock the instrument into its normal operating position on the rack:

a. Slide two self-anchoring #10-32 tinnerman nuts on the mounting-rail of the rack (each side). These nuts should be aligned with the angle-bracket slots. Omit the tinnerman nuts if the mounting-rail is tapped for #10-32 screws

b. Slide the instrument fully into the rack until the angle brackets strike the slide-mount bracket screws. Secure the instrument in place using four phillips panhead #10-32 x 3/4 screws

2.6 MISCELLANEOUS OPTION INSTALLATION

2.6.1 Rear-Panel Input Option 01

2.6.1.1 Refer during this procedure to Figure 2.7A, B, and C as well as Option 01 Assy Drawing 404378 in Section 7. The installation package includes:

a. Rear-Input Option Assy PCB (1)

b. Rear-Input 72-conductor Cable Assy (1)

c. Phillips panhead self-locking #6-32 X .312 screws (9)

d. Metal blind-threaded #6 standoffs (5)

2.6.1.2 Complete the following steps:

a. Loosen, but don't remove, the two rear corner-feet by unfastening the four retaining screws (two per foot). Back the corner feet out approximately 5/8 inch. This permits removal of the top and bottom covers

b. Slide both the top and bottom covers toward the rear of the unit, then lift up and out to remove

c. Turning counterclockwise, remove the lock nuts from the front-panel BNC connectors for INPUTs A and B (attached to the signal conditioner board) and INPUT C

d. Remove the black rear-hole plug from J210 on the 1996. Remove INPUT C's BNC connector with its cable from the front panel and install in J210 on the rear panel of the 1996. Place the rear-hole plug for INPUT C on the front panel

e. Remove the five self-locking screws from the top of the signal conditioner board. These screws fasten the signal conditioner PCB to the motherboard. Set these screws aside

f. On the 1995, disconnect the 2-conductor (black & white, twisted-pair) 10 MHz internal frequency reference and 14-conductor twisted-wire power cables connecting the signal conditioner PCB and motherboard. This involves unplugging P8 from J8 (10 MHz cable) and P6 from J6 (power cable) on the signal conditioner board. In addition, on the 1996, unplug P7 from J7 on the signal conditioner board. This disconnects the other 2-conductor (black & white, twisted-pair) 10 MHz internal frequency reference cable. P17/J17, P18/J18 (1996), and P19/J19 can remain connected on the motherboard during this procedure. Set the free ends of the three disconnected cable assemblies safely aside for later reconnection.

g. Slide the signal conditioner board towards the rear of the instrument; pull the board up and remove, setting it aside

h. Remove the two black rear-hole plugs from J201 and J202 and place them on the front panel

i. Place the Option 01 assembly board into the unit, center slot towards the rear. Connect P9A on the option board and J9 on the motherboard

j. Fasten the option board securely to the motherboard using the existing four short standoffs and four self-locking screws

k. Tip the instrument on its side. Insert and securely fasten the five supplied long metal standoffs to the motherboard using five self-locking screws, inserting them from the bottom of the unit through the motherboard

l. Connect the rear-input option ribbon cable to the option board using plug P9B and socket J9B. Fold the cable halfway back towards the rear of the unit

m. Reverse the signal conditioner board 180° (INPUT A and B connectors towards the rear panel) and hold the board in one hand. Connect the other end of the rear-input option cable to the bottom of the signal conditioner board using plug P9 and socket J9A

n. Align INPUT A and B BNC connectors on the signal conditioner board with their corresponding rear-panel holes, then slide the board so that these connectors protrude through the holes

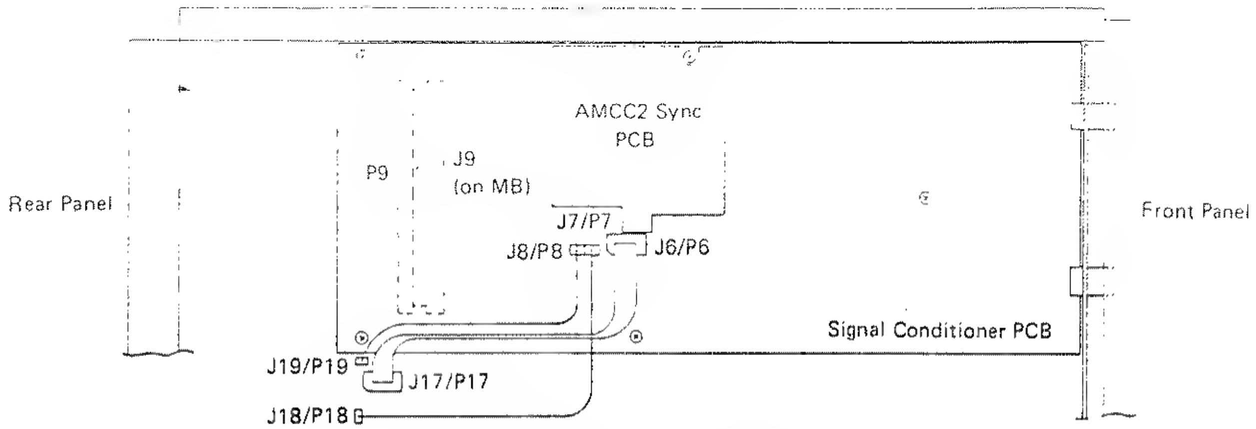
o. Orient the signal conditioner board so that its five holes align with the five longer standoffs just fastened to the motherboard. Secure the signal conditioner board to these standoffs using the original five self-locking screws, inserting them through the top of the board

p. Secure the BNC connectors for all rear-mounted inputs using their lock nuts.

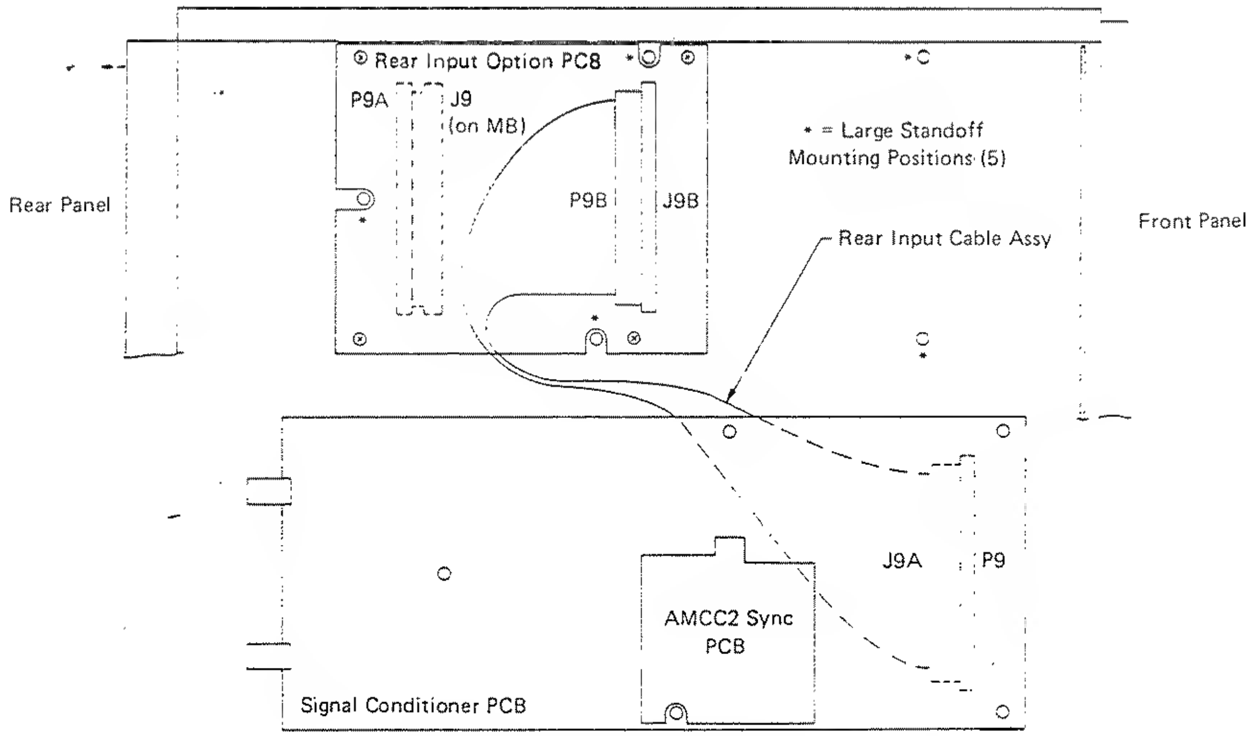
q. Reconnect the single black & white 10 MHz internal frequency reference (two on the 1996) and power cable assemblies to the signal conditioner board as before

r. Replace the top and bottom covers; firmly secure the two rear corner-feet, completing the installation

(A) - Front Input Configuration



(B) - Option 01 PCB Installation



(C) - Rear Input Configuration

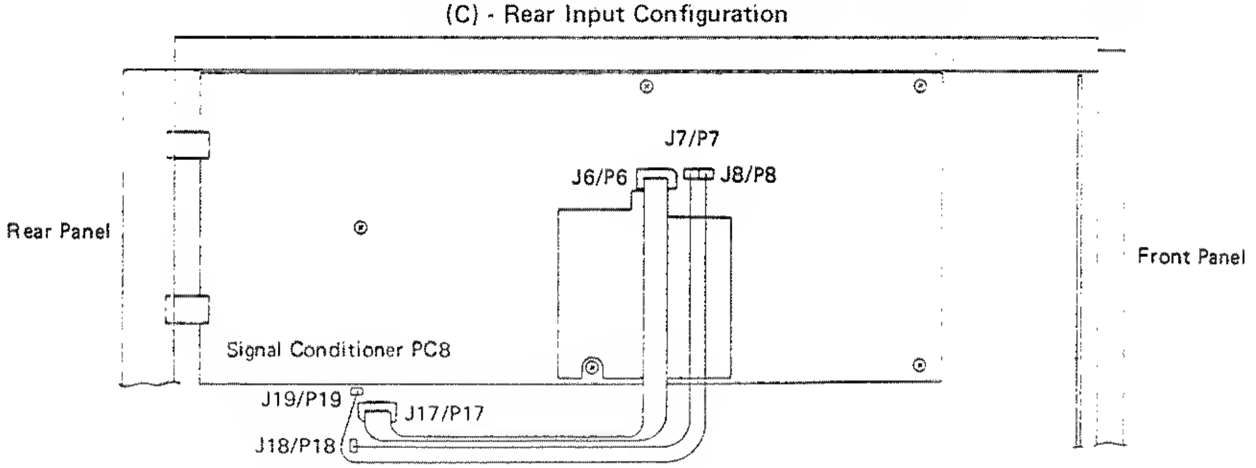


Figure 2.7-Rear-Panel Input (Option 01) Installation

2.6.2 High-Stability Oven Oscillator Option 04E

2.6.2.1 Refer to Figure 2.8 for this procedure. The installation package includes:

a.	Oscillator assembly (1)	P/N 404386 for Option 04E
b.	#4 split lock washers (2)	P/N 617127
c.	#4 flat washers (2)	P/N 617102
d.	M3 x 8 screws (2)	P/N 611067
e.	Cable tie (1)	P/N 610777

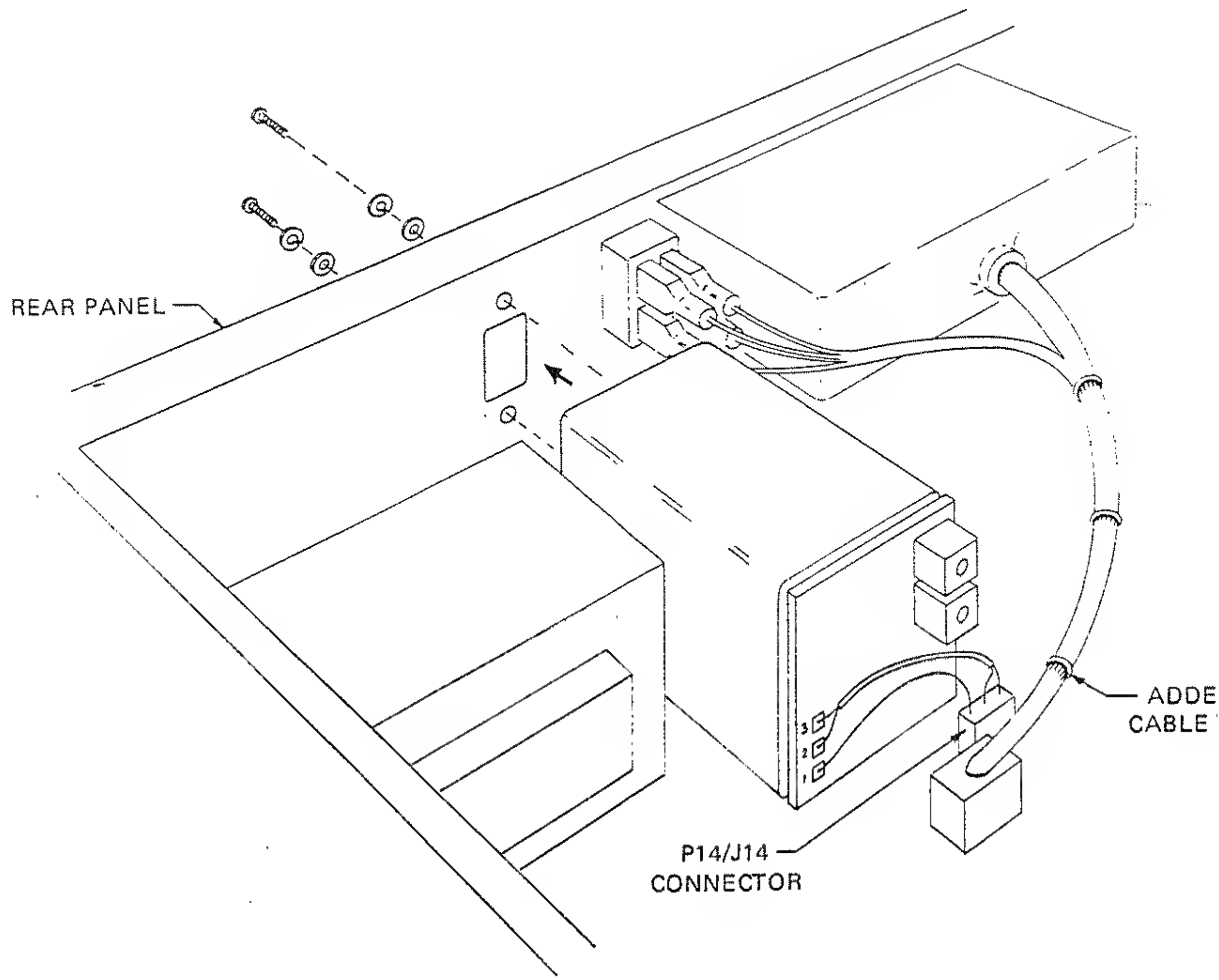


Figure 2.8 - Option 04E Installation

2.6.2.2 Installation

a. Disconnect the AC power cord at the rear panel

b. Loosen, but don't remove, the two rear corner-feet by unfastening the four retaining screws (two per foot). Back the corner feet out approximately 5/8 inch. Slide the top cover toward the rear of the unit, then lift up and out to remove

c. Remove the currently fitted standard 10 MHz oscillator assembly by:

   1. Removing the cable tie securing cables to P14/J14 and P13/J13

   2. Extracting the two screws and washers attaching the oscillator assembly to the rear panel via the two threaded standoffs

   3. Disconnecting the 5-pin connector cable (P14) from the motherboard at J14, then lifting the oscillator assembly out of the chassis

d. Connect the 5-pin connector cable of the option oscillator assembly at J14 on the motherboard

e. Replace the cable tie securing cable to P13/J13

f. Secure the oscillator assembly to the rear panel using the two M3 x 8 screws, two flat washers, and two lock washers. The screws pass directly into the top of the oscillator assembly

g. Replace the top cover; firmly secure the two rear corner-feet, completing the installation

2.7 POWER CONNECTIONS

2.7.1 Before operating the counter, verify that the AC voltage selector is correctly set for the local AC supply. The counter operates on 100, 120, 220, or 240 volts, 50 to 60 Hz. The present voltage range can be seen through the small window in the power input module on the rear panel.

2.7.2 Line Voltage Selection

2.7.2.1 The line voltage setting is easily changed by repositioning the small voltage selector card in its slot. Refer to Figure 2.9 and use the following procedure:

a. Remove the power cord from the power input module

b. Fully slide the transparent fuse cover to the left. This exposes the fuse and voltage selector card

c. Pull the small lever marked FUSE PULL completely to the left. This ejects the fuse from its holder, permitting access to the selector card

d. Remove the selector card, then reposition it in its slot so that the desired line voltage designation is visible. (Using a small pair of needle-nose pliers can be helpful in completing this step.)

e. Pull the lever completely back to the right, snapping it closed

f. Replace the fuse in it holder. Line voltage settings of 100 or 120V should have a 1A Slow-Blow fuse installed; settings of 220 or 240V should have a .5A Slow-Blow fuse installed.

g. Slide the fuse cover completely to the right covering the voltage selector card and fuse. The correct line voltage designation should be visible through the window

h. Connect the power cord to the counter again

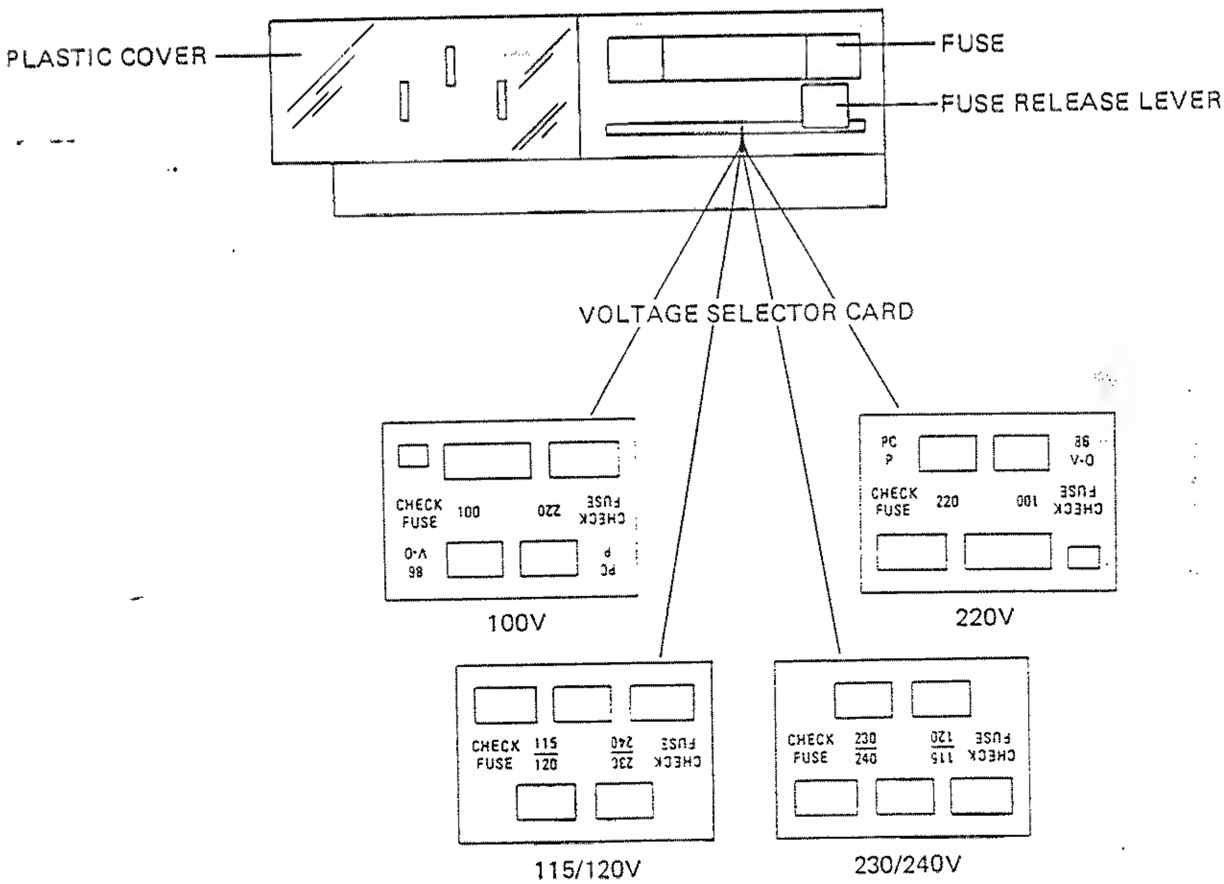


Figure 2.9 - AC Line Voltage Selection

2.7.3 Power Cord and Grounding

2.7.3.1 The front panel and instrument case are grounded in accord with MIL-T-28800C protecting the user from possible injury due to shorted circuits.

NOTE

Both counters are designed to meet IEC Publication 348, "Safety Requirements for Electronic Apparatus for Class I Instruments."

2.7.3.2 A protective ground terminal, forming part of the rear-panel input socket, i provided. Both counters are supplied with a detachable 3-core power cord. Only this cor should be used.

2.7.3.3 Use only AC power outlets having a protective ground for connection to the counter. **DO NOT USE** 2-core extension cords or 3-prong to 2-prong adapters that don't provide a protective ground connection. Connection of the power cord to the power outlet must be made in accordance with the following standard color code:

	American	European
Live	Black	Brown
Neutral	White	Blue
Ground (Earth)	Green	Green/Yellow

2.7.3.4 Also, all devices connected to or in proximity with the 1995/1996 must maintain the third-wire ground(earth) intact as set forth in current regulations.

2.8 STORAGE AND TEMPERATURE

2.8.1 The 1995/1996 can be stored at temperatures ranging from -40°C to +70°C at 75% relative humidity without adverse effects to PCBs or components. The counter must be brought within its specified operating range of 0°C to +50°C before power-on.

2.9 FUNCTIONAL CHECK

2.9.1 Introduction

2.9.1.1 The following test procedure confirms whether or not the 1995/1996 is performing correctly by checking most of the counter's circuitry. This procedure should be conducted when the 1995/1996 is first put into service and after shipment to a new location.

2.9.1.2 Now perform the following procedure:

a. Connect the 1995/1996 to a suitable AC power supply

b. Turn on the rear-panel power switch. It should illuminate. Confirm that the front-panel POWER (ON/STBY) button is out (⊥) and the STBY LED lit

c. Depress the front-panel POWER (ON/STBY) button to ON, supplying power to the entire counter. Verify that the STBY LED turns off

d. Confirm that the instrument model number "1995" or "1996" is displayed for about two seconds, and then the main display blanks

NOTE:

Home-state conditions for the 1995/1996 are listed in Subsection 3.2.3. Refer as required.

e. Provide a 50Ω coaxial test lead fitted with BNC connectors. This lead should be 60 cm to 1 m long

f. Using the test lead, connect the 10 MHz REF-OUT connector (see Figure 3.2) on the rear panel to Input A's connector

NOTE:

After power-on, the following home-state conditions exist: FREQ A, AUTO-TRIG A, X1, 1 MΩ, AC-coupling, Filter off, and COM A off.

g. Verify that the main display shows 10.000000 ± 1 count E6 Hz; that both the GATE and Input A TRIG LEDs flash

h. Select Input B using key sequence <21> SHIFT STORE SF SHIFT SF. Verify that the SF LED is lit

i. Using the same coaxial test lead, connect the 10 MHz REF-OUT connector to Input B's connector

j. Repeat step g for Input B

k. Toggle the SF key using key sequence SHIFT SF. The SF LED should turn off

l. Disconnect the test lead between the REF-OUT and Input B connectors

m. If the counter is Model 1996, select FREQ C. Connect the test lead between the REF-OUT and Input C connectors

n. Verify that the main display shows 10.000000 ± 1 count E6 Hz and that the GATE LED flashes

3.1 INTRODUCTION

3.1.1 This section contains information for operating the 1995/1996 as a bench instrument. It provides General Operating Information, Front and Rear Panel Descriptions, and Operating Procedures.

3.2 GENERAL OPERATING INFORMATION

3.2.1 If the counter is being used for the first time or at a new location, ensure that the voltage selector is set for the correct local AC supply before turning on the instrument. Refer to Subsection 2.7.2, as required, for details on line voltage selection.

3.2.2 Power-On and Self Test

3.2.2.1 Turn on the rear power switch, placing the counter in the Standby mode. The front-panel STBY LED should be lit if the red POWER-ON button is out (▲). In Standby, power is supplied to the instrument's frequency standard (timebase). This eliminates the need for warmup each time the 1995/1996 is turned on.

3.2.2.2 Depress the POWER-ON/OFF button to its ON (▁) position. Power should now be supplied to the entire counter and the STBY LED should be off.

3.2.2.3 After powering-on, the 1995/1996 executes a programmed self-test of the major internal circuitry. This check verifies normal operation of the counter's microcomputer, counting circuitry, timebase, and ROM memory circuitry. Should a failure occur during this self-test, a numbered error is displayed.

3.2.3 Home State

3.2.3.1 After self-test, the counter reverts to a home state, ready for operation. The following home-state conditions are selected after "self-test":

a. AUTO-TRIG A enabled; AUTO-TRIG B disabled

b. Time Interval DELAY: 1 millisecond. (Verify using key sequence SHIFT RECALL DELAY)

c. GATE Time: ten milliseconds. (Verify using key sequence SHIFT RECALL GATE)

d. Math constants X, Y and Z: 0, 1 and 1, respectively. (The value for scale constant Z should never be zero.)

e. FREQ A

f. Slope A (positive); Slope B (negative)

g. Attenuation: X1 (Input A); X50 (Input B)

h. Input impedance: 1 MΩ

i. Separate inputs (i.e., Common A LED is off)

j. Filter: off

k. Hysteresis: 25 mV p-p (lower value)

l. Sample(n) value: 100

m. Input A and B trigger levels: Zero (relevant only if auto-trigger is not selected)

n. Input Coupling: AC-coupled (Inputs A and B)

3.2.4 Main Display

3.2.4.1 Readings are displayed in engineering format with a 10-digit mantissa, 1-digit exponent, and floating decimal point. It is assumed that the reading is positive unless (1) the negative-sign LED to the left of the display is lit, or (2) a negative sign precedes the displayed mantissa. Keyboard entries are always right-justified. The largest displayed reading is 999.9999999 with a +9 exponent; the smallest number is 1.000000000 with a -9 exponent. The 1-digit exponent range is -9 to +9.

3.2.4.2 The selected function and gate time determine the number of digits displayed. Generally, the longer the gate time, the more digits displayed. The RESOLUTION (↑↓) keys are used to either step the gate time up (to 100 seconds), increasing the number of digits displayed; or down (to 200 nanoseconds), decreasing the number of digits displayed.

3.2.4.3 LED indicators for units in Hz (hertz) and S (seconds) are located at the right of the exponent display. Units for some functions are implied. For example, phase angle measurements are in degrees. Seven LEDs (O/F, REM, ADDR, SRQ, EXT ARM, EXT STD, and GATE) are situated immediately below the display (see Table 3.1).

3.2.5 Keyboard Organization

3.2.5.1 The front panel of the 1995/1996 is arranged logically by function into color-coded keyboard/LED groups. Refer to the front-panel figures and Table 3.1 for location and description. Listed below (left to right) are the keyboard groups with their color coding indicated in parentheses:

a. General Operating (gray)

b. FUNCTION (yellow)

c. INPUT C (1996 only-blue)

d. DATA ENTRY (brown)

e. INPUT A (blue)

f. Input Control (gray)

g. INPUT B (blue)

3.3 PANEL DESCRIPTIONS

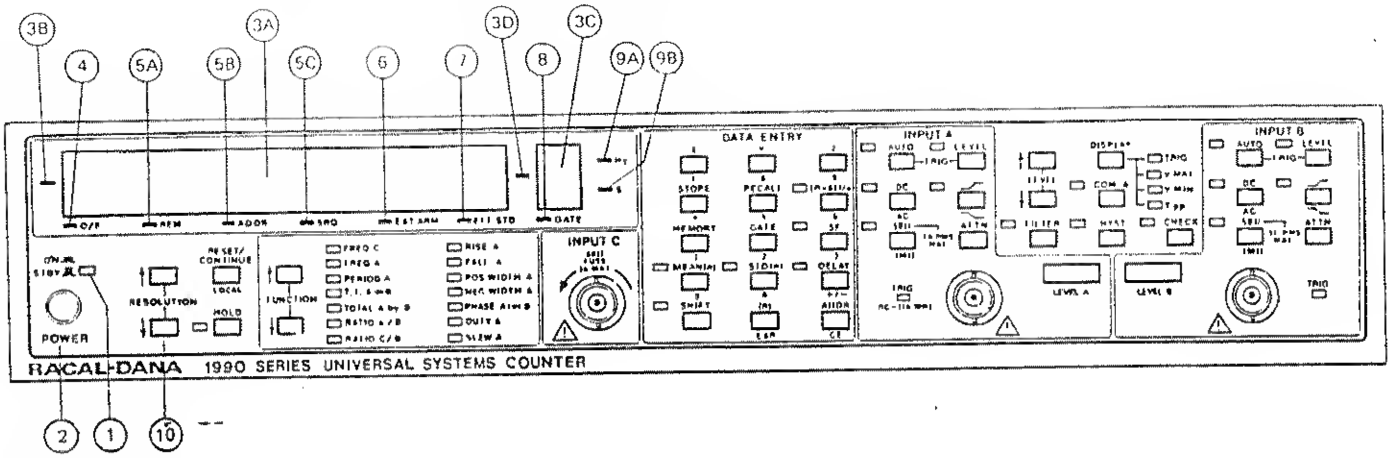
3.3.1 Front Panel Features

3.3.1.1 Refer to Table 3.1 and the front-panel figures. They show and describe front-panel controls, indicators, and connectors.

NOTE:

In the following table, LEDs shown in the "Item" column with an asterisk (*) are described in their lit condition. Certain LEDs are associated with toggle keys; their lit condition is specified.

Table 3.1 - Front-Panel Controls, Indicators, and Connectors

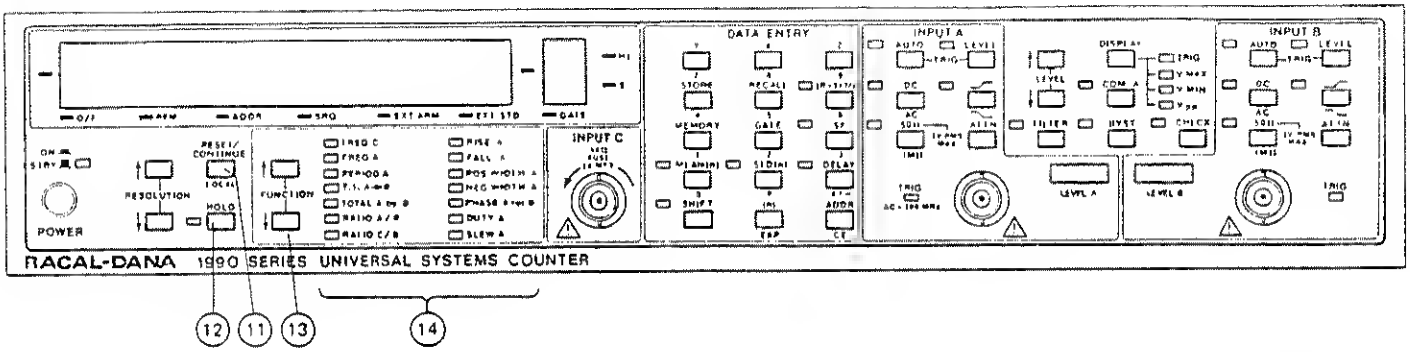


Reference	Item	Function/Description
1	STBY LED*	In Standby. Rear-panel POWER switch is on, front-panel POWER (ON/STBY) button is out, and power is supplied only to the internal reference standard (timebase)
2	POWER (ON/STBY) Button	In ON position, power is supplied to the entire counter and the STBY LED is off
3	Measurement Display:	A 7-segment LED digital display. Uses engineering format with 10-digit mantissa, 1-digit exponent, and floating decimal point. The display shows one of the following depending on operational state: _____ measurement results _____ numbers for data entry _____ numbers for recall from constant or function stores _____ error messages NOTE: The exponent LED is blanked and should be considered zero during the following: a. phase measurement b. totalize measurement with less than ten digits c. numeric entries not involving an exponent
3A	Mantissa Display LEDs*	Display right-justified mantissa
3B	Mantissa Sign LED*	Negative display number
3C	Exponent Display LED*	One-digit exponent number
3D	Exponent Sign LED*	Negative exponent

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)

Reference	Item	Function/Description
4	O/F LED*	Readout overflows the tenth digit of the display
5	GPIB LEDs:	
5A	REM LED*	Counter under remote control over the GPIB interface
5B	ADDR LED*	Counter is being addressed as either a talker or listener over the GPIB interface
5C	SRQ LED*	Counter has transmitted a service request over the GPIB interface
6	EXT ARM LED*	External arming is controlling the measurement start and stop points
7	EXT STD LED*	Counter is operating from an external frequency standard reference
8	GATE LED*	Measurement gate is operating, starting or stopping a measurement cycle
9	Display Units LEDs:	**NOTE:** Neither LED lights when a phase angle, ratio, totalize measurement, or a constant is displayed
9A	Hz LED*	Units in Hertz for a frequency measurement
9B	S LED*	Units in Seconds for a time measurement
10	RESOLUTION Keys (↑↓)	Step the measurement period (i.e., gate time and also the resolution) either up (↑) or down (↓). This increases or decreases the number of digits displayed. In Recall Special Function mode, the lowest special function number is initially displayed. Use the RESOLUTION (↑↓) keys to scroll (with wrap-around) through special function numbers on display

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)



Reference	Item	Function/Description
11	RESET/CONTINUE, LOCAL Key	This key provides the following: **RESET** Terminates the measurement in progress, clears the main display, and triggers a new measurement **NOTE:** In HOLD mode, pressing this key triggers a new measurement cycle **CONTINUE** Returns the counter to the measurement mode, triggers a new measurement cycle, after the display of recalled number or constant **LOCAL** Returns the counter to front-panel control from remote control on the GPIB, provided local lock-out has not been set
12	HOLD Key/LED	Toggles counter in and out of HOLD (single-shot measurement). LED lights in HOLD. In HOLD, the measurement in progress is completed and displayed. See NOTE under Reference 11 . Special Function 61 causes the HOLD key to successively start and stop measurements for manual Totalize
13	FUNCTION Keys (↑ ↓)	Select in succession the counter's measurement function. The corresponding FUNCTION LED is lit. Function selection "wraps around" at both ends

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)

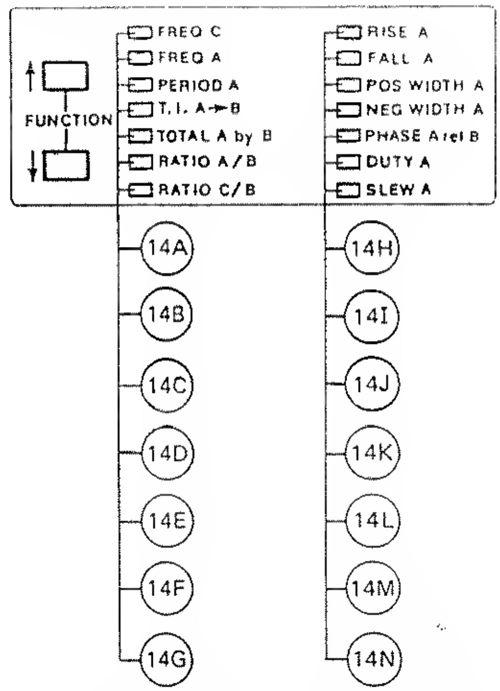
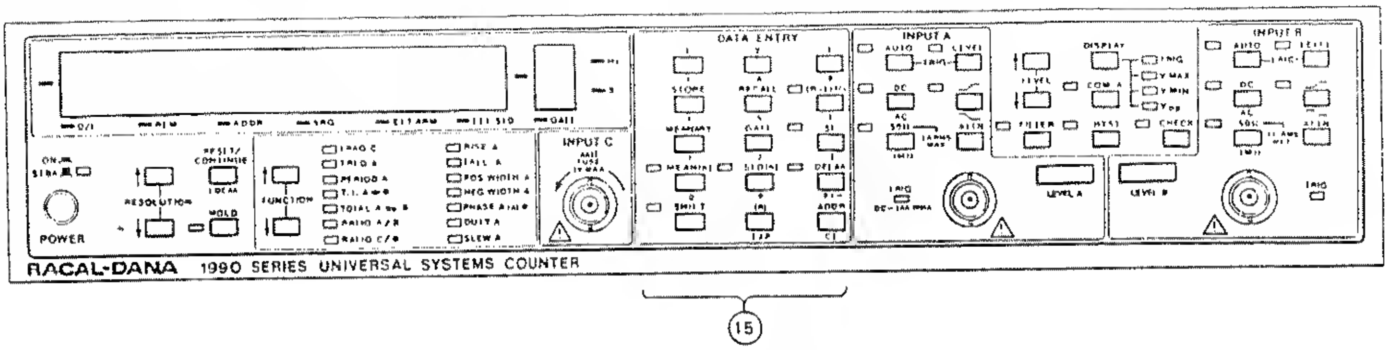
Reference	Item	Function/Description
14	FUNCTION LEDs:	Indicate selected function 
14A	FREQ C*	Input C Frequency (1996 only)
14B	FREQ A*	Input A Frequency
14C	PERIOD A*	Input A Period
14D	TI A→B*	Time Interval (Input A for start, Input B for stop)
14E	TOTAL A by B*	Totalize (Input A events gated by Input B)
14F	RATIO A/B*	Ratio A/B (Ratio of Frequency A to Frequency B)
14G	RATIO C/B*	Ratio C/B (Ratio of Frequency C to Frequency B)
14H	RISE A*	Input A Rise Time (10% start, 90% stop trigger points)
14I	FALL A*	Input A Fall Time (90% start, 10% stop trigger points)
14J	POS WIDTH A*	Input A Positive Pulse-Width (50% trigger points)
14K	NEG WIDTH A*	Input A Negative Pulse-Width (50% trigger points)
14L	PHASE A rel B*	Phase difference (Input A relative to Input B)
14M	DUTY A*	Input A Duty Cycle
14N	SLEW A*	Input A Slew Rate (positive/negative, 20% to 80% trigger points)

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)



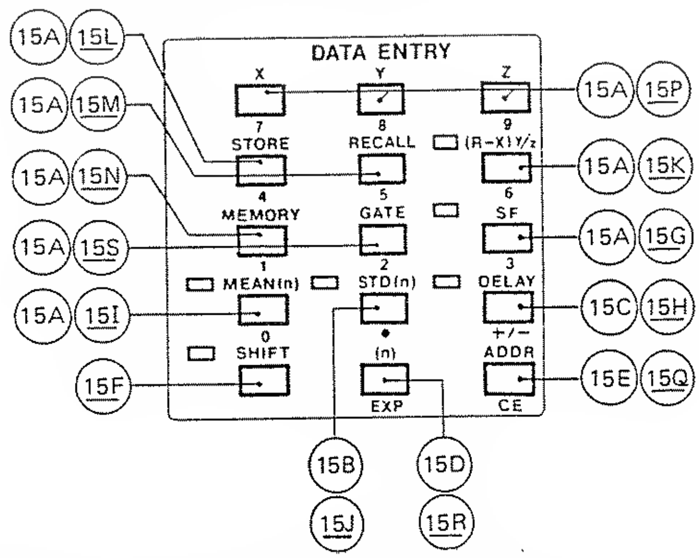
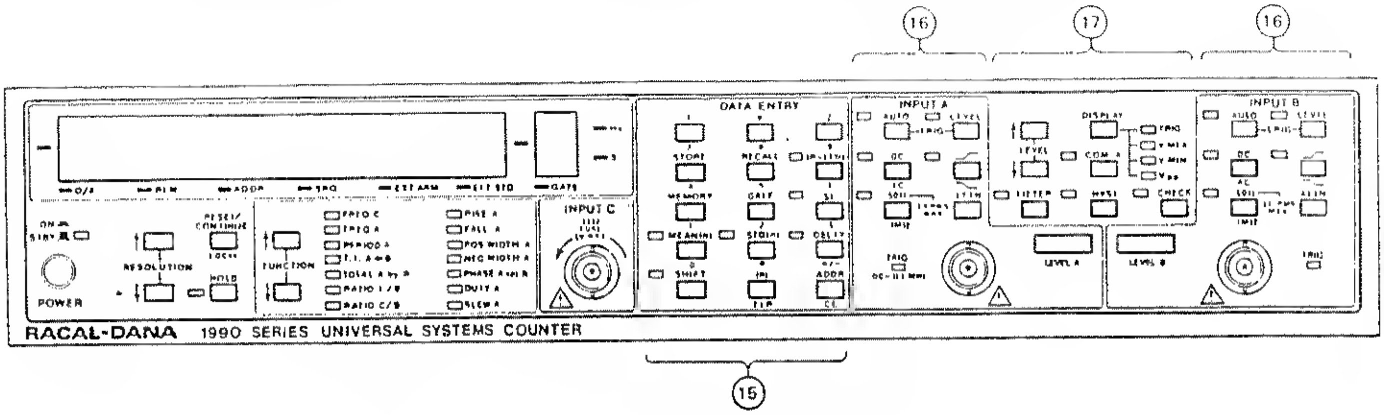
Reference	Item	Function/Description
15	DATA ENTRY Keys/LEDs **NOTE:** Designators for shifted key functions are underlined. Also, designator "15O" is not used	Permit data entry and user interface with the 1995/1996 other than input signal conditioning and measurement functions 
15A	Unshifted Key functions: Numeric Keys (0-9)	Entry of numbers and constants for math, special functions, time-interval stop delays, trigger levels, and gate times. Also, used to recall machine setups. When a numeric key is pressed, the measurement in progress is aborted and the display shows the entered number
15B	Decimal Point (.) Key	Inserts decimal point during numeric entry
15C	Positive/Negative (+/-) Sign Key	Toggles sign of entered number (mantissa and/or exponent) between positive (no sign displayed) and negative (sign displayed)
15D	EXP Key	Changes data entry mode so that the next number entered is the exponent

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)

Reference	Item	Function/Description
15E	CE Key	Clears current display number and entry
15F	Shifted Key Functions: SHIFT Key/LED*	Enables any shifted key function. After pressing a shifted key function (except for STORE, RECALL, and MEMORY), counter immediately returns to its unshifted state with the SHIFT LED turning off
15G	SF Key/LED*	Enables all selected special functions (SHIFT SF). Also stores (<NN> SHIFT STORE SF) and recalls (SHIFT RECALL SF) special functions. See Subsection 3.4.8 for details
15H	DELAY Key/LED*	Enables a time-interval stop delay (SHIFT DELAY) in TI A→B. Also, stores (<value> SHIFT STORE DELAY) and recalls (SHIFT RECALL DELAY) a time-interval stop delay. Enabling a delay in a non- TI function produces an error message. Selecting a non-TI function when in delay disables DELAY and turns off the LED
15I	MEAN(n) Key/LED*	Enables calculation and display of the mean (average) of (n) samples. Pressing SHIFT MEAN(n) deselects the STD(n) key if enabled. Pressing RESET restarts the period of (n) samples
15J	STD (n) Key/LED*	Enables calculation and display of the standard deviation of (n) samples. Pressing SHIFT STD(n) deselects the MEAN(n) key if enabled. Pressing RESET restarts the period of (n) samples
15K	(R-X) Y/Z Math Key/LED*	Selection of Math computation mode
15L	STORE Key	Stores constants for math functions, gate time, time-interval delay, (n) samples, GPIB address and special functions. Used with MEMORY key to store complete measurement (i.e., machine) setups
15M	RECALL Key	Recalls constants for math functions, gate time, time-interval delay, (n) samples, GPIB address and special functions and calibration. Used with MEMORY key to recall complete measurement (i.e., machine) setups
15N	MEMORY Key	Store and recall complete measurement setups, memory locations 0 to 9, and calibration constants, locations 10 to 33 (see Table 3.16). Use the key sequence SHIFT STORE/RECALL MEMORY<N>. Attempted store or recall of an out-of-range number produces an error message

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)



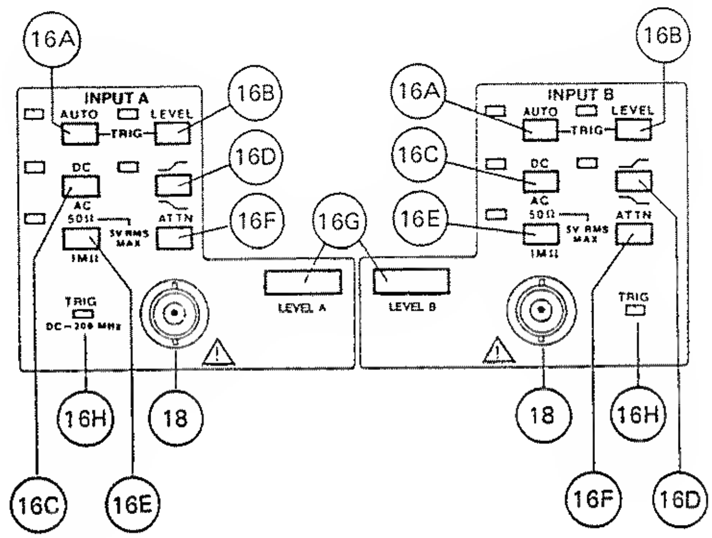
Reference	Item	Function/Description
15P	X/Y/Z Keys	Store and recall Math computation constants (X, Y and Z)
15Q	ADDR Key	Store and recall the counter's GPIB address. Address procedure is shown on rear panel (see Table 3.2) to the right of the GPIB connector
15R	(n) Key	Store and recall of (n) samples for statistics. Range of (n) is 2 to 9999
15S	GATE Key	Store and recall gate time
16	INPUT A and B Keys/ LEDs	
16A	AUTO-TRIG Keys/LEDs*	Automatic trigger setting and tracking for Inputs A and B
16B	TRIG-LEVEL Keys/LEDs*	Manual trigger setting for Inputs A and B
16C	DC/AC Keys/LEDs*	Toggle between DC/AC input coupling for Inputs A and B. LED lit when DC-coupled

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)

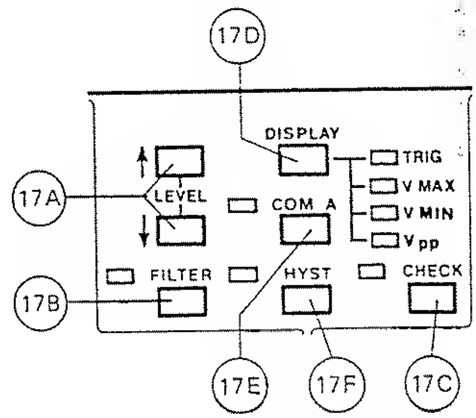
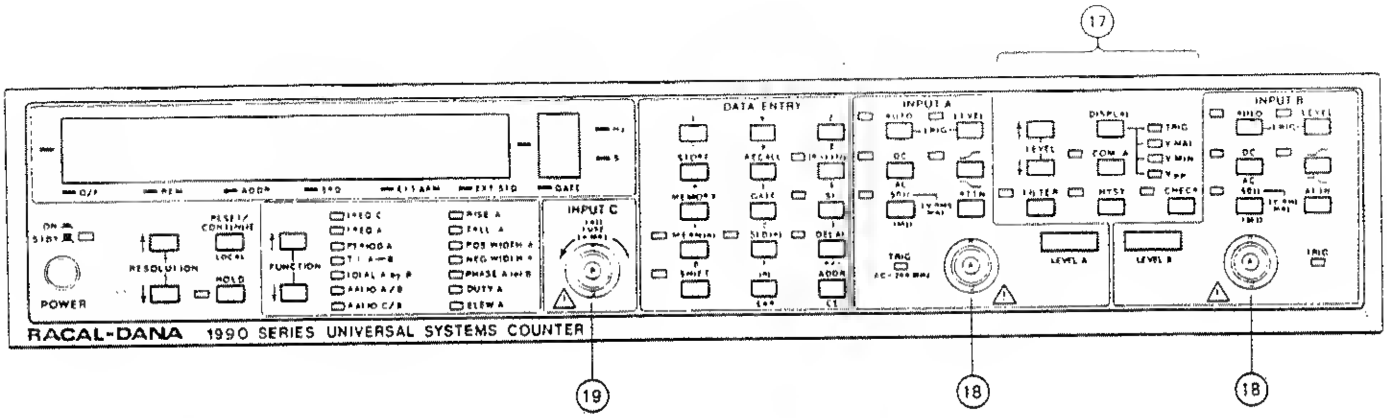
Reference	Item	Function/Description
16D	╱/╲ Keys/LEDs*	Toggle between positive (╱) and negative (╲) trigger slopes of Inputs A and B. LED lit in positive slope
16E	50Ω/1MΩ Keys/LEDs*	Toggle between 50Ω and 1MΩ input impedance for Inputs A and B. LED lit in 50Ω mode
16F	ATTN (X1, X10, X50) Keys	Attenuation for Inputs A and B. The decimal point shifts in the LEVEL A and B displays, indicating attenuation range selected (X1=X.XX, X10=XX.X, and X50=XXX.)
16G	LEVEL A and B Displays	Indicate current trigger level (manual or auto-trigger). LEVEL A and LEVEL B also show TRIG (current trigger level), V MAX, V MIN, and Vpp when selected using the DISPLAY key 17D
16H	TRIG LEDs/Inputs A and B	Flash to indicate input signal is triggering measurement circuits
17	INPUT CONTROL Keys/LEDs*	Control Input A and B signals NOTE: LEVEL ↑↓ keys have no LED indicators 
17A	LEVEL ↑ ↓ Keys	Step manually-set trigger levels either up (↑) or down (↓) in increments of 0.01, 0.1, or 1 volts for the X1, X10, and X50 attenuation ranges, respectively. Use key sequence TRIG-LEVEL LEVEL ↑↓ TRIG-LEVEL
17B	FILTER Key/LED	Toggles a low-pass input filter (100 kHz cutoff frequency) for Inputs A and B. LED lights when filter is on. Special Functions 28 and 29 permit separate filter selection for Inputs A and B, respectively

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)



Reference	Item	Function/Description
17C	CHECK Key/LED	Verifies the proper operation of front-panel LEDs and executes internal self-tests. Pressing the CHECK key lights the CHECK LED immediately. However, the CHECK key must be held down about 3 seconds for all LEDs to light, all 8's to display, and the self-test functions to be executed. Release of the CHECK key extinguishes all LEDs and displays the word "TEST", indicating the unit is under self-test. When all self testing is completed the unit displays 5 MHz. Toggle the CHECK key to turn off the CHECK LED. Momentarily pressing the CHECK key will simply cause the counter to measure an internal 5 MHz test waveform
17D	DISPLAY Key/LEDs:	Scrolls through TRIG, V MAX, V MIN, and Vpp. Values are displayed in LEVEL A and LEVEL B
	TRIG *	Current trigger level
	V MAX *	Maximum peak voltage
	V MIN *	Minimum peak voltage
	Vpp *	Voltage peak-to-peak
17E	COM A Key/ LED	Toggles Input A also to B. LED lit in COM A mode
17F	HYST Key/LED	Toggles the hysteresis level for Inputs A and B between a low (25 mVpp) and high (100 mVpp) setting. HYST LED lights in the higher setting
18	INPUT(s) A and B	BNC connectors for INPUT(s) A and B. INPUT A is used for all functions except Frequency C (1996 only). INPUT B is used with INPUT A for Time Interval, Ratio A/B, Totalize, and Phase measurements. INPUT B is used with INPUT C for Ratio C/B. Special Function 21 internally exchanges INPUTS A and B (providing, e.g., FREQ B, etc. measurement capability)

Table 3.1 - Front-Panel Controls, Indicators, and Connectors (Con't)

Reference	Item	Function/Description
19	INPUT C (1996 only)	BNC connector high-frequency INPUT C (40 MHz-1.3 GHz range). INPUT C is used with INPUT B for Ratio C/B. Special Function 21 provides Ratio C/A capability. Protection against excessive signal levels (>5V rms) is provided by a fuse in the input socket

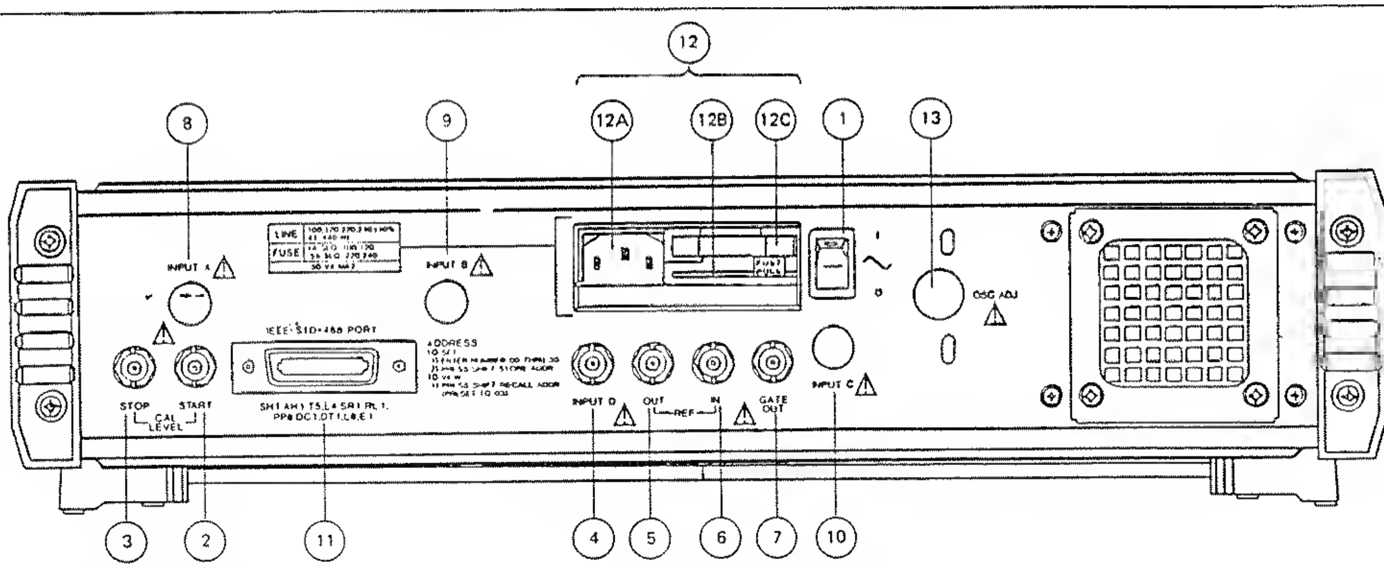
NOTE:

In the above table, LEDs shown in the "Item" column with an asterisk (*) are described in their lit condition. Certain LEDs are associated with toggle keys; their lit condition is specified.

3.3.2 Rear-Panel Features

3.3.2.1 Refer to Table 3.2 and figure at top. They indicate and briefly describe the rear-panel controls and connectors.

Table 3.2 - Rear-Panel Controls and Connectors



Reference	Item	Function/Description
1	Main Power Switch	Enables Standby if the front panel POWER (ON/STBY) button is out (■). This supplies power to the internal frequency standard (timebase). Also, switches counter ON/OFF if front-panel POWER (ON/STBY) button is in (▬)
	NOTE: Connectors 2 through 10 are BNCs	
2	START-CAL LEVEL Connector	Output: analog signal equivalent of the Start trigger level (for calibration only)
3	STOP-CAL LEVEL Connector	Output: analog signal equivalent of the Stop trigger level (for calibration only)
4	INPUT D Connector	Input: external arming/gating control signal
5	REF-OUT Connector	Output: 10 MHz internal reference
6	REF-IN Connector	Input: external reference frequency (1,5, or 10 MHz at 1V rms)
7	GATE OUT Connector	Output: negative-going TTL-compatible signal equivalent to the gate signal

Table 3.2 - Rear-Panel Controls and Connectors (Con't)

Reference	Item	Function/Description
8	INPUT A Connector (Option 01)	Rear-panel Input A
9	INPUT B Connector (Option 01)	Rear-panel Input B
10	INPUT C Connector (Option 01) **NOTE:** Front-panel INPUTS A, B, and C are not connected when Option 01 is installed. Input is only via the rear-panel connectors	Rear-panel Input C
11	GPIB Connector	GPIB (IEEE-STD-488-1978) connector
12	Power Input Module:	
12A	AC Power Input Socket	Standard connector for the AC power supply
12B	Line Voltage Selector	Small printed circuit card inserted in module to select correct AC line voltage. The selected voltage (100, 120, 220, or 240 VAC) is visible through the small window
12C	Line Fuse	A glass cartridge Slow-Blow fuse. Line fuse ratings for available line voltages are shown on the upper-left of the rear-panel
13	OSC ADJ	Adjustment of the internal reference frequency standard

3.4 OPERATING PROCEDURES

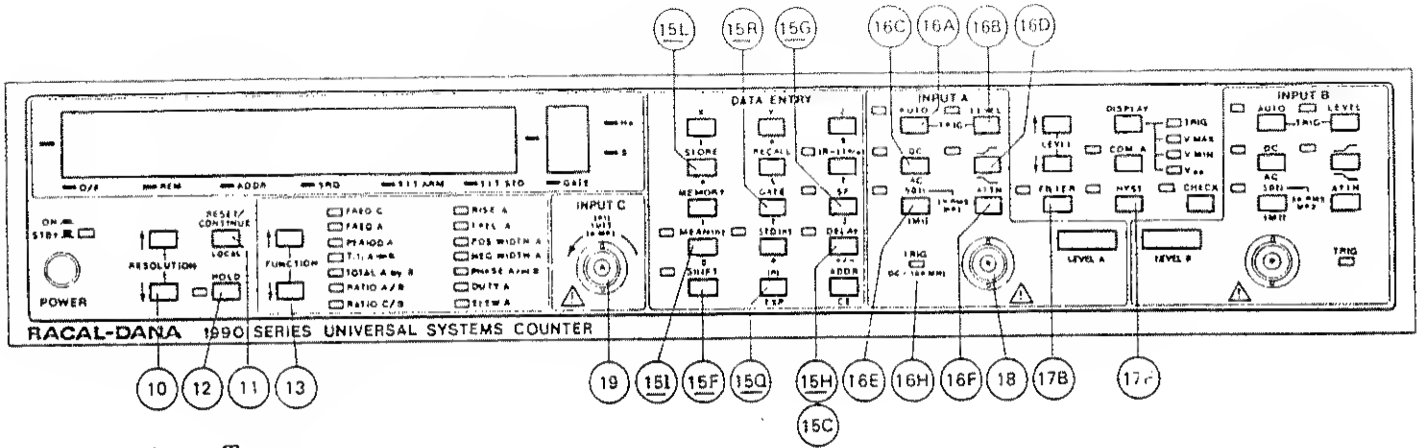
3.4.1 Measurement Functions

3.4.1.1 Tables 3.3-3.13 with figures describe the basic bench functions of the 1995/1996.

NOTE:

Review as required Table 3.1, References 18 and 19, for use of Inputs A, B, and C, including Special Function 21 permitting interchange of Inputs A and B. See also Subsection 3.4.8 and Table 3.14 for special functions.

Table 3.3 - Frequency Measurement



1. --Turn power on.

2. Select FREQ A or FREQ C (1996 only) using FUNCTION keys (13).

3. If FREQ A is selected, set the AC/DC coupling (16C) and input impedance (16E) as required.

4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the measurement signal to INPUT A (DC to 200 MHz) (18) or INPUT C (40 MHz to 1.3 GHz) (19).

6. If a specific gate time is desired, enter it (in seconds, using the exponential format for small values) using key sequence <value>SHIFT (15F) STORE (15L) GATE (15R) . Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓ keys (10) to select the required display resolution and gate time if step 6 was not used.

8. If FREQ A is selected, either set the trigger level manually using key sequence <value>+/- (15C) TRIG-LEVEL (A) (16B), or select AUTO-TRIG (A) (16A) . Check that Input A TRIG LED (16H) flashes.

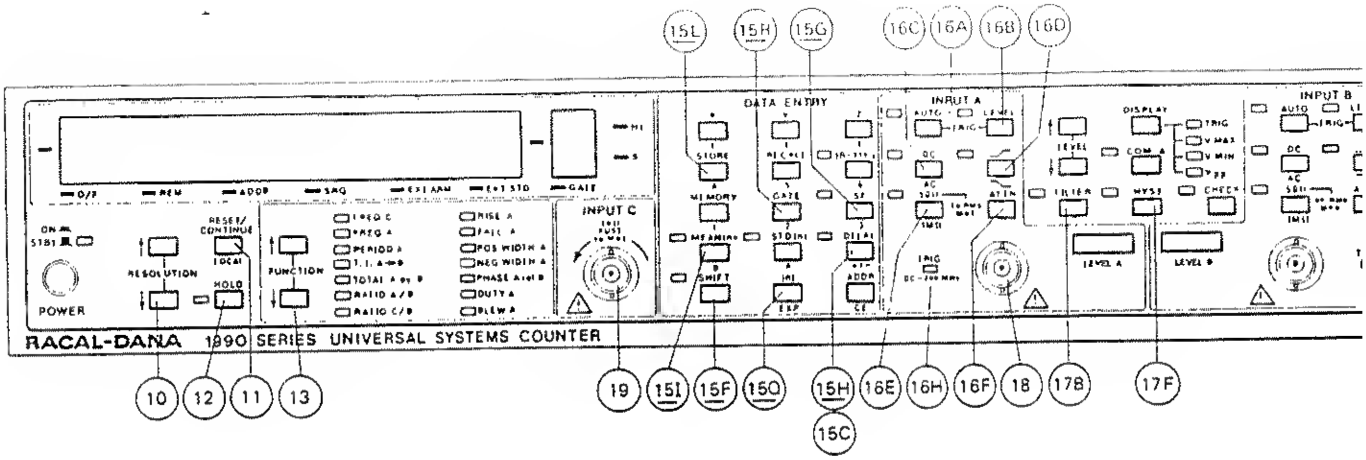
9. If a frequency below 100 kHz is to be measured in the presence of high frequency noise, select the FILTER (17B).

10. Set the input hysteresis (17F) at low or high as required. The high setting may be used to filter low-frequency noise.

11. If external arming/gating is needed, connect the arming/gating signal and select the special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

12. Select the Hold mode (12) for single-shot measurements. Press the RESET (11) while in Hold to trigger a new measurement.

Table 3.4 - Period Measurement



1. Turn power on.

2. Select PERIOD A using FUNCTION keys (13).

3. Set the AC/DC coupling (16C) and input impedance (16E), as required.

4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the measurement signal to INPUT A (18).

6. If a specific gate time is desired, enter it (in seconds using the exponential format for small values) using key sequence <value>SHIFT (15F) STORE (15L) GATE (15R). Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓ keys (10) to select the required display resolution and gate time if step 6 was not used.

8. Either set the trigger level manually using key sequence <value> +/- (15C) TRIG-LEVEL (A) (16B), or select AUTO-TRIG (A) (16A). Check that Input A TRIG LED (16H) flashes.

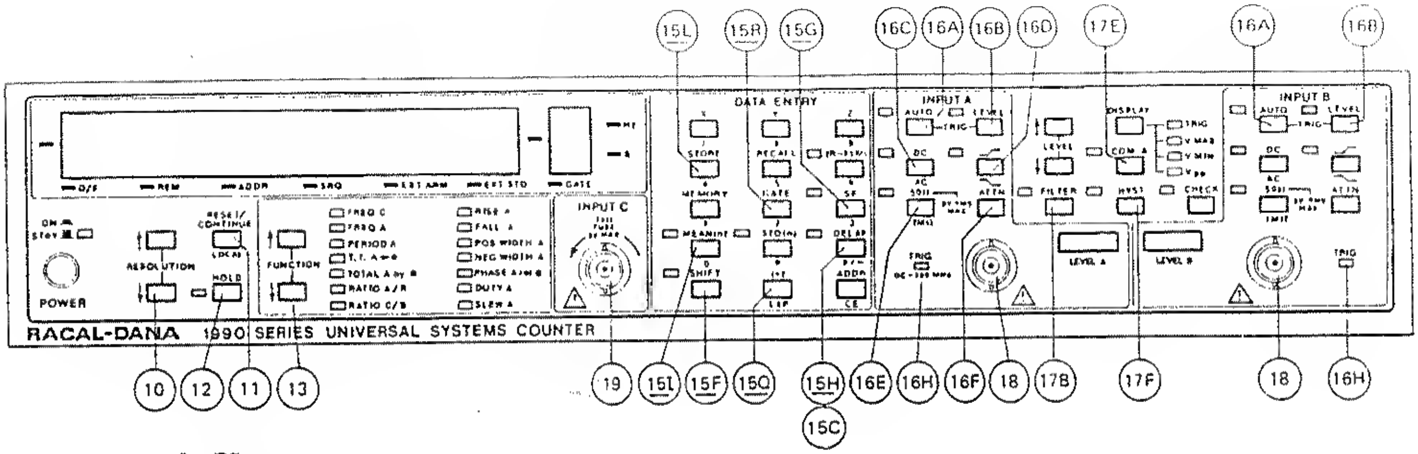
9. If a frequency below 100 kHz is to be measured in the presence of high frequency noise, select the FILTER (17B).

10. Set the input hysteresis (17F) at low or high as required. The high setting may be used to filter low-frequency noise.

11. If external arming/gating is needed, connect the arming/gating signal and store the special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

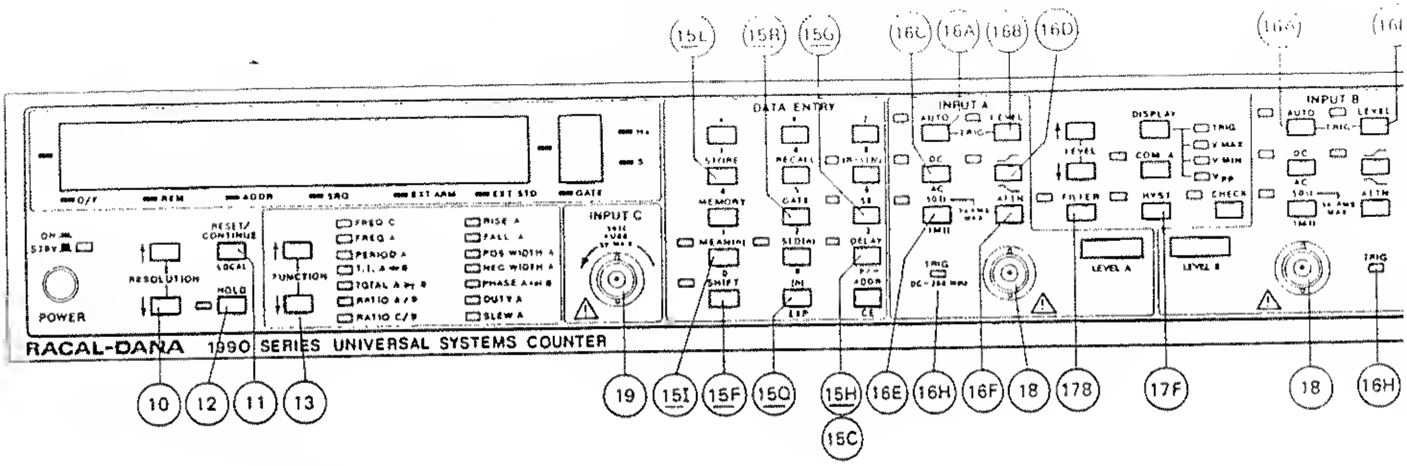
12. Select the Hold mode (12) for single-shot measurements. Press the RESET (11) while in Hold to trigger a new measurement.

Table 3.5 - Time Interval Measurement



1. Turn power on.
2. Select TI A→B using FUNCTION keys (13).
3. Set AC/DC coupling (16C), input impedance (16E), and slope (16D) for Inputs A/B as required. If the start and stop signals are from the **same source**, select COM A (17E).
4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.
5. Connect the start signal to INPUT A (18). If a separate source for the stop signal is used, connect the stop signal to INPUT B (18).
6. Either set the trigger levels A/B manually using key sequence <value>+/- (15C) TRIG-LEVEL (16B), or select AUTO-TRIG A/B (16A). Check that Inputs A and B TRIG LEDs (16H) flash.
7. Set the input hysteresis (17F) at low or high as required.
8. If internal delayed arming of the stop circuit is required, enter the delay into memory using key sequence <value> SHIFT (15F) STORE (15L) DELAY (15H). Enable the delay using key sequence SHIFT (15F) DELAY (15H).
9. If external arming/gating is needed, connect the arming/gating signal and store the special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.
10. Select the Hold mode (12) for single-shot measurements. Press the RESET (11) while in Hold to trigger a new measurement.

Table 3.6 - Total A by B Measurement



1. Turn power on.

2. Select TOTAL A by B using FUNCTION keys (13).

3. Set AC/DC coupling (16C), input impedance (16E), and slopes (16D) as required.

4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

NOTE:

Input A slope selects the slope of the events to be totalized. The measurement period, however, starts on Input B slope and stops on the opposite slope.

5. Connect the signal to be totalized to INPUT A (18) and the control signal to INPUT B (18).

6. Either set the trigger levels A/B manually using key sequence <value>+/- (15C) TRIG-LEVEL (16B), or select AUTO-TRIG A/B (16A). Check that Inputs A and B TRIG LEDs (16H) flash.

7. If a frequency below 100 kHz is to be measured in the presence of high-frequency noise, select the filter (17B).

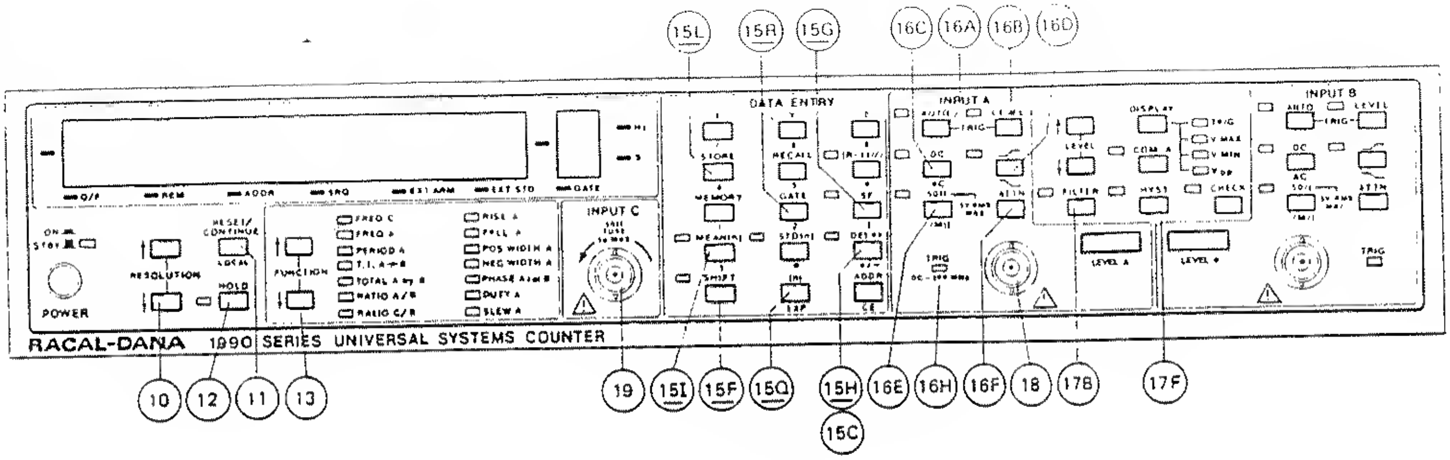
8. Set the input hysteresis (17F) at low or high as required. The high setting may be used to filter low-frequency noise.

9. If internal delayed arming of the stop circuit is required, enter the delay into memory using key sequence <value>SHIFT (15F) STORE (15L) DELAY (15H). Enable the delay using key sequence SHIFT (15F) DELAY (15H).

10. If external arming/gating is needed, connect the arming/gating signal and store the special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

11. Select the Hold mode (12) if necessary. Press the RESET (11) while in Hold to trigger a new measurement.

Table 3.7 - Manual Totalize Measurement



1. Turn power on. Select TOTAL A by B using the FUNCTION keys (13).

2. Set AC/DC coupling (16C), input impedance (16E), and slope (16D) for Input A as required.

3. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

4. Enter Special Function 61 using key sequence 61 SHIFT (15F) STORE (15L) and SF (15G). Enable special functions using key sequence SHIFT (15F) SF (15G).

5. Connect the measurement signal to INPUT A (18).

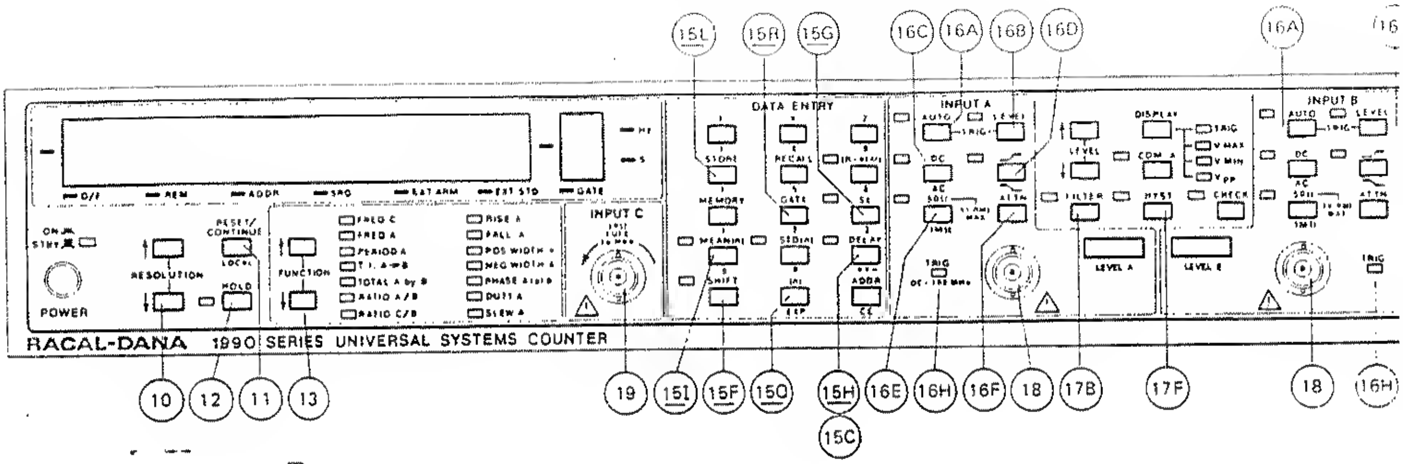
6. Either set trigger level A manually using key sequence <value> +/- (15C) TRIG-LEVEL (16B), or select AUTO-TRIG A (16A). Check that Input A TRIG LED (16H) flashes.

7. If a frequency below 100 kHz is to be measured in the presence of high-frequency noise, select the filter (17B).

8. Set the input hysteresis (17F) at low or high as required. The high setting may be used to filter low-frequency noise.

9. Operate the HOLD key (12). Verify that the count stops. The displayed result is cumulative over successive measurement cycles. Use the RESET key (11) to clear the display. Check that the main display blanks before triggering new measurement cycles.

Table 3.8 - Ratio A/B and C/B Measurements



1. Turn power on.

2. Select RATIO A/B or RATIO C/B (1996 only) using FUNCTION keys (13).

3. Set AC/DC coupling (16C), input impedance (16E), and slope(s) (16D) as required.

4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect one signal to INPUT B (18) and the other to INPUT A (18) or INPUT C (19). The lower frequency signal should be connected to INPUT B.

6. If a specific gate time is desired, enter it (in seconds, using the exponential format for small values) using key sequence <value> SHIFT (15F) STORE (15L) GATE (15R). Skip step 7 if step 6 is being used to enter the gate time.

7. Use the RESOLUTION ↑↓keys (10) to select the required display resolution.

8. If RATIO A/B is selected, either set trigger levels A/B manually using key sequence <value> +/- (15C) TRIG-LEVEL (16B), or select AUTO-TRIG A and B (16A). Check that Inputs A and B TRIG LEDs (16H) flash. For RATIO C/B, a trigger level for only INPUT B may be specified.

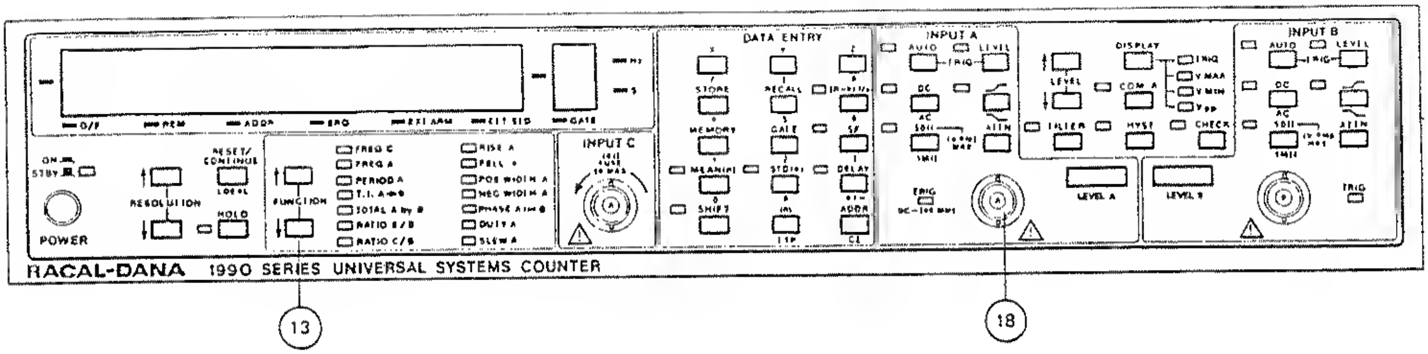
9. If a frequency below 100 kHz is to be measured in the presence of high frequency noise, select the filter (17B).

10. Set the input hysteresis (17F) at low or high as required.

11. If external arming/gating is needed, connect the arming/gating signal and select the special function number. Enable special functions. Refer to Subsection 3.4.8 for special function numbers and procedures.

12. Select the Hold mode (12) for single-shot measurements. Press the RESET (11) while in Hold to trigger a new measurement.

Table 3.9 - Positive/Negative Pulse Width Measurements

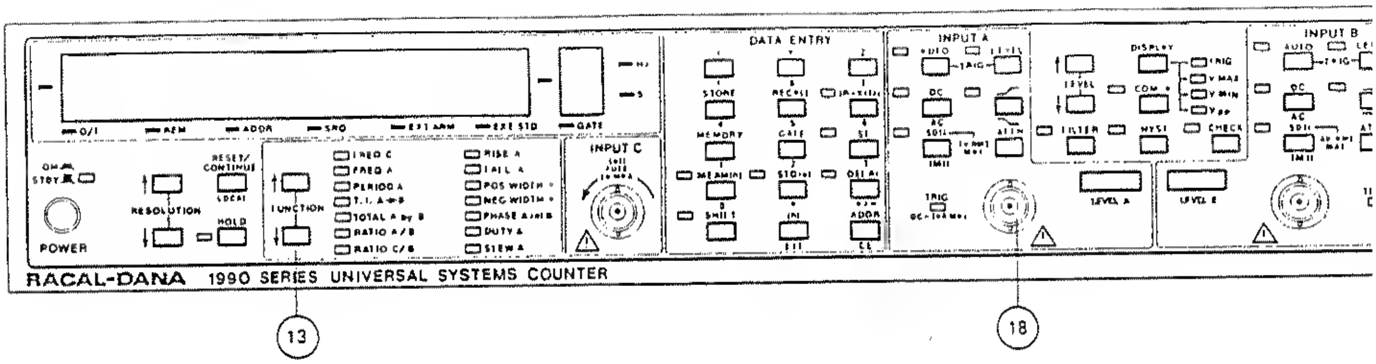


1. Turn power on.
2. Select either POS WIDTH A or NEG WIDTH A using FUNCTION keys (13).
3. Connect measurement signal to INPUT A (18).

NOTE:

All other controls are set automatically.

Table 3.10 - Rise A/Fall A Measurements

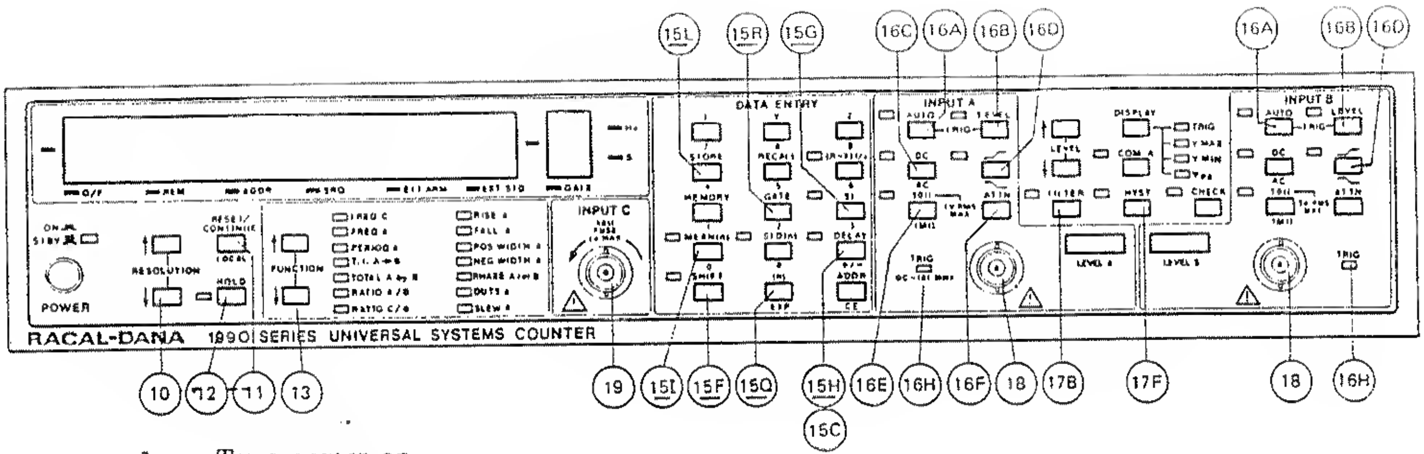


1. Turn power on.
2. Select either RISE A or FALL A using FUNCTION keys (13).
3. Connect measurement signal to INPUT A (18).

NOTE:

All other controls are set automatically.

Table 3.11 - Phase A rel B Measurement



1. Turn power on.

2. Select PHASE A rel B using FUNCTION keys (13).

3. Select AC/DC coupling (16C), input impedance (16E), and slopes (16D) as required. Selected slopes for signals A and B should be the same.

4. Select the X10 or X50 input attenuation (16F) if desired. Attenuation setting is automatic in the Auto-Trigger mode.

5. Connect the signals to be compared to INPUT A and INPUT B (18).

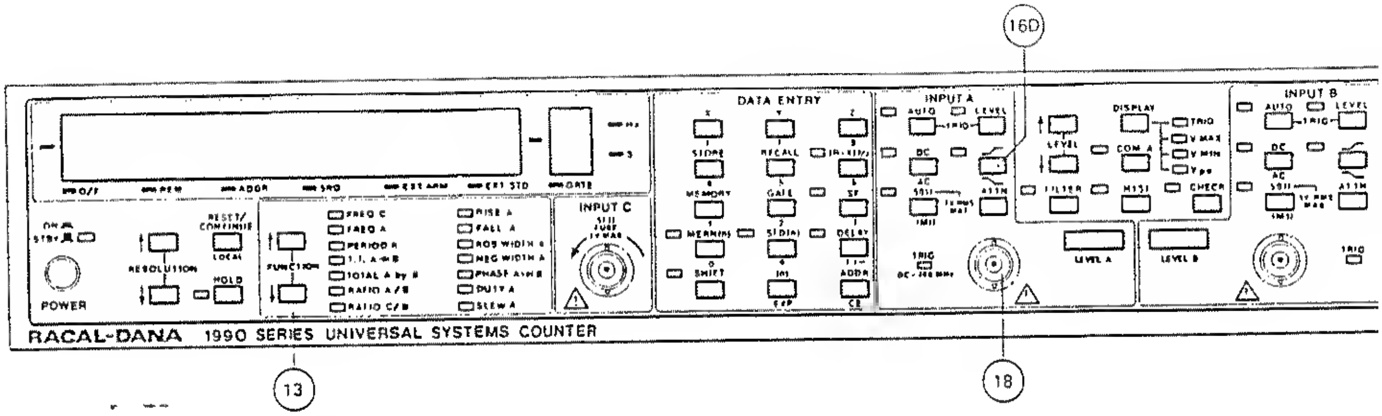
6. Either set the trigger levels A/B manually using key sequence <value> +/- (15C) TRIG-LEVEL (16B), or select AUTO-TRIG A/B levels (16A). Check that Inputs A/B TRIG LEDs (16H) flash.

7. Select the Hold mode (12) for single-shot measurements. Press the RESET (11) while in Hold to trigger a new measurement.

NOTE:

A phase measurement is always positive, representing the angle by which Input A's signal leads that of Input B. The signals for phase measurement must be continuous and have the same frequency.

Table 3.12 - Duty A Measurement

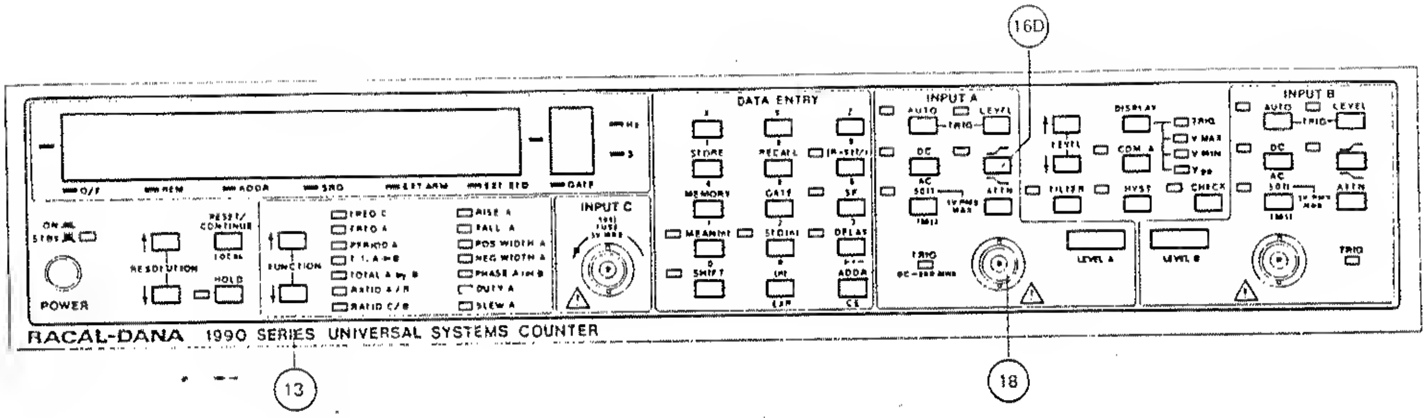


1. Turn power on.
2. Select DUTY A using FUNCTION keys (13).
3. Select the slope (16D) as required.
4. Connect the signal to INPUT A (18).

NOTE:

All other controls are set automatically.

Table 3.13 - Slew A Measurement



1. Turn power on.
2. Select SLEW A using FUNCTION key (13).
3. Select the slope (16D) as required.
4. Connect the signal to INPUT A (18).

NOTE:

All other controls are set automatically.

3.4.2 Trigger Level Setting

3.4.2.1 Introduction

3.4.2.1.1 Refer to Figure 3.1 for this subsection. The 1995/1996 both provide manual a automatic (including single-shot) trigger setting for Inputs A and B. Manual trigger select involves setting the levels in ±5V, ±50V, and ±250V ranges, with corresponding resolutions of mV, 100 mV, and 1V. These ranges correspond to attenuation settings of 1X, 10X, and 50X a LEVEL A and B trigger displays of X.XX, XX.X, and XXX., respectively. Auto-Trigger level the mean of the positive and negative-peak values of the input signal as automatica determined by the counter.

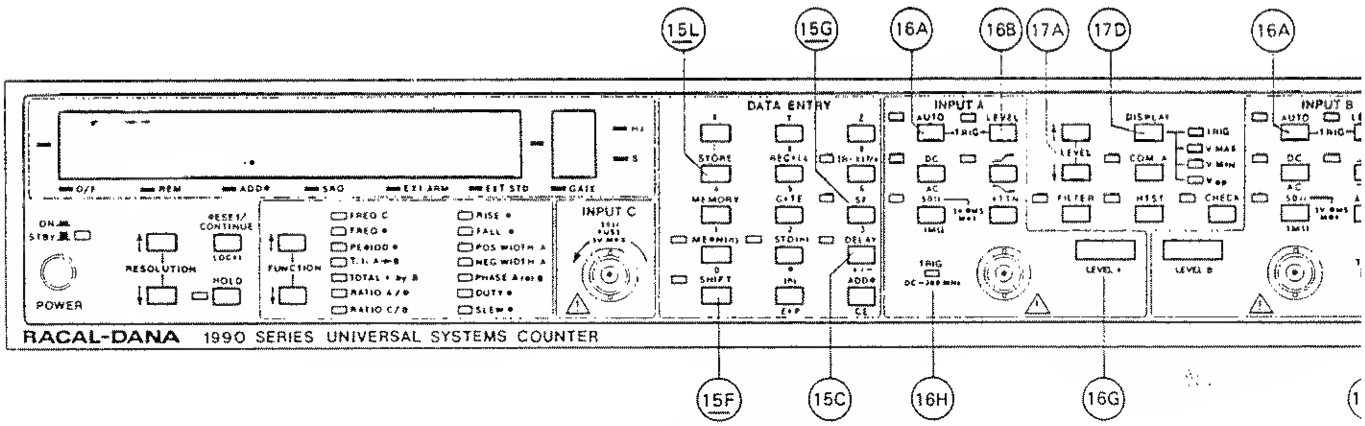


Figure 3.1 – Trigger Level Setting

3.4.2.2 Manual Trigger Setting

NOTE:

An attenuation setting of X1 and a trigger level of 1.23 volts are used in the following description.

3.4.2.2.1 Set the trigger level manually using one of the following key sequences:

a. For setting a +1.23, use <1.23> TRIG-LEVEL (16B)

b. For setting a -1.23, use +/- (15C) <1.23> TRIG-LEVEL (16B)

3.4.2.2.2 After entering a manual trigger level, it is continuously displayed on the LEVEL A/LEVEL B LED(s) (16G). The 1995/1996 returns immediately to its measurement mode after trigger setting. TRIG A/TRIG B LED(s) (16H) flash if the counter is triggered from the input signal.

3.4.2.2.3 Use key sequence TRIG-LEVEL (16B) LEVEL↑↓ (17A) TRIG-LEVEL (16B) to step the displayed trigger level up or down by 0.01 (X1), 0.1 (X10), or 1. (X50) as required. Verify the trigger level changes on the LEVEL A/LEVEL B LED(s) (16G).

3.4.2.2.4 A manual trigger level that is out-of-range for the current attenuation setting produces an error message.

NOTE:

INPUT A and B each have one trigger-level store. Using the Auto-Trigger mode overwrites a manually stored trigger setting. Also, pressing the AUTO-TRIG key (16A) while manually setting the level enables the Auto-Trigger mode. Toggle the AUTO-TRIG key (16A) off, then enter a manual trigger level.

3.4.2.2.5 Press the DISPLAY key (17D) to show V MAX, V MIN or Vpp of the input signal in the LEVEL A/LEVEL B display.

3.4.2.3 Automatic Trigger Setting

3.4.2.3.1 Press the required AUTO-TRIG key (16A) to calculate and show the trigger level in the LEVEL A/LEVEL B display. Automatic attenuation setting occurs in the Auto-Trigger mode.

3.4.2.3.2 Press the DISPLAY key (17D) to show V MAX, V MIN, or Vpp of the input signal in the LEVEL A/LEVEL B display.

3.4.2.4 Single-Shot Automatic Trigger

3.4.2.4.1 Automatic trigger settings vary as peak input levels change. To execute and store a single-shot Auto-Trigger level:

a. Enter Special Function 31 using key sequence 31 SHIFT (15F) STORE (15L) and SF (15G)

b. Enable special functions using key sequence SHIFT (15F) SF (15G)

c. Press the AUTO-TRIG key (16A). The LED lights as the level is calculated and set, then turns off.

3.4.2.4.2 The stored level is retained as a manually set value until either (1) another single-shot measurement is made, or (2) a new manual trigger level is entered.

3.4.2.4.3 To execute additional single-shot trigger settings, press the AUTO-TRIG key (16A) again with Special Function 31 enabled.

3.4.3 Gate Time and Resolution

3.4.3.1 Frequency Functions

3.4.3.1.1 Gate Time Mode - by specifying the counter's gate time, the user can set the resolution in the frequency, period, and ratio functions. Gate times from 200 ns to 100s may be selected. To enter a gate time, use the key sequence <value> SHIFT STORE GATE where <value> is either in decimal or exponential form. To recall a gate time for display, use the key sequence SHIFT RECALL GATE. Use the RESOLUTION↑↓keys to decadically step the displayed gate time (and resolution) either up(↑) towards 100 s or down (↓) towards 200 ns. The counter's gate time (and resolution) can be set to display from one to ten digits (with overflow).

EXAMPLE

Assume FREQ A is selected and a 1 ms gate time specified. Successively pressing the RESOLUTION (↑) key will select and display gate times (and resolutions) of 10 ms, 100 ms, 1s, 10s, and 100s. Successively pressing the RESOLUTION (↓) key will select and display gate times (and resolutions) of 100 µs, 10 µs, and 1 µs. Pressing the RESOLUTION (↓) key again after displaying 1 µs will not produce a gate time of 100 ns as this value is smaller than the 200 ns lower gate-time limit. The 1 µs will continue to display on the counter.

3.4.3.1.2 Resolution Mode - when no gate time is specified in frequency, period, and ratio functions, the counter's resolution can be selected using the RESOLUTION (↑↓) keys. Now the gate time is automatically set via the number of displayed digits of resolution. Except in some Math computations, pressing the RESOLUTION (↑↓) keys will increment/decrement the display by one digit per keyboard maneuver. Each digit displayed decadically increases/decreases the counter's resolution within the counter's gate time range. Gate times from 200 ns to 100 s may be selected. There will be no step-up or-down when the RESOLUTION (↑↓) keys are pressed in Time Interval, Totalize, Rise/Fall Time, Positive/Negative Pulse Width, or Slew Rate functions.

EXAMPLE

A 9-digit resolution of a measurement is possible in a 1-second gate time; 10-digit resolution in a 10-second gate time; and 10-digit resolution plus overflow in a 100-second gate time. If one selects a gate time which sets a resolution exceeding the 10-digit display resolution, then an overflow of the most significant digit(s) and lighting of the O/F LED occurs. Two overflow states are permitted in the 1995/1996. In an overflow condition, the user can reduce the gate time to display any "dropped" digit(s). Digits that overflow are not lost, but remain stored in the counter's registers for output over the GPIB.

3.4.3.2 Time Functions

3.4.3.2.1 In Time Interval functions (TI A→B, Rise/Fall, and Pulse Width, e.g.,), the input signal is synchronized with the measurement gate. Thus, there is no gate time as such. The input signal, therefore, determines the counter's resolution. On the 1995/1996, a single-shot Time Interval resolution to 1 ns is possible.

3.4.4 Delay Mode

3.4.4.1 When Time Interval (TI), Totalize, or Positive/Negative Pulse Width is selected, an internal delay from 200 ns to 100 s may be entered from the front panel. This permits the user to increase the elapsed time between the start and stop trigger points by the gate time range. Once stored, the delay may be enabled/disabled as required. Use of the Delay mode prevents premature triggering from spurious signals during measurement.

3.4.4.2 The delay is stored using either an exponential or decimal format. Use one of the following key sequences to store, for example, a 1 μs delay:

a. 1 EXPONENT +/- 6 SHIFT STORE DELAY

b. <.000001>SHIFT STORE DELAY

NOTE:

Once the delay is entered, the counter returns to the measurement mode.

3.4.4.3 Recall the delay to the main display using key sequence SHIFT RECALL DELAY.

3.4.4.4 Enable and disable a stored delay by successively using key sequence SHIFT DELAY. The LED lights when the Delay mode is enabled.

3.4.5 Arming/Gating Selection

3.4.5.1 Refer to Table 3.14 as required. External arming, external gating, and synchronous window auto-trigger (Syn. Wind. AT) modes are selectable via special functions for Inputs A, B, or D.

3.4.5.2 External Arming

3.4.5.2.1 Special Functions 82.0 through 83.3 as applied to the external arming input (A, B, or D) permit selection of positive or negative start edges in the 1995/1996.

3.4.5.3 External Gating

3.4.5.3.1 Special Functions 85.0 through 88.3 as applied to external gating inputs (A, B, or D) permit selection of positive or negative start/stop edges in the 1995/1996.

3.4.5.4 Synchronous Window Auto-Trigger (Syn. Wind. AT)

3.4.5.4.1 Special Functions 91.0 through 94.3 as applied to the external arming input (A, B, or D) permit selection of positive or negative start/stop edges in the counter. Auto-trigger can establish the positive/negative signal peak measurements and trigger level only during the time when the Syn. Wind. AT signal is present. The auto-trigger can now be used for display of peak voltage values of a specific pulse(s) selected by the operator using the Syn. Window AT signal.

3.4.6 Math Function (R-X)Y/Z

3.4.6.1 The Math function applies to all counting and timing functions of the 1995/1996 except phase measurement. This function permits measurement value R to be offset, normalized, and/or scaled before display using stored constants X, Y, and/or Z, respectively. The display indicates (R-X)Y/Z after enabling the Math function. Home state values for X, Y, and Z are 0, 1, and 1, respectively ($Z \neq 0$ at any time).

3.4.6.2 Math Constant Storage

3.4.6.2.1 Constants X, Y, and/or Z must be stored before enabling the Math function. Use key sequence <value> SHIFT STORE X/Y/Z, where <value> is in decimal or exponential form, to enter any of the constants. The permissible range of values for the Math constants is ± 0.000000001E-9 to ± 9999999999E9. Any number exceeding this range will result in "Error 20" being displayed.

3.4.6.3 Math Constant Recall

3.4.6.3.1 Recall stored Math constants to the main display using key sequence SHIFT RECALL X/Y/Z.

3.4.6.4 Math Function Enabling/Disabling

3.4.6.4.1 Enable and disable the Math function by successively using key sequence SHIFT (R-X)Y/Z. The LED lights when the Math function is enabled.

3.4.7 Statistical Functions/(n) Samples

3.4.7.1 The 1995/1996 Statistical functions include the Mean, Standard Deviation, and Low/High values for user-entered (n) samples. Mean and Standard Deviation are enabled using single front-panel keys; Low/High values by special functions.

3.4.7.2 (n) Samples

3.4.7.2.1 The range of (n) samples is any positive integer from 2 to 9999 (fractions entered for n are truncated). Home state value for (n) samples is 100.

3.4.7.2.2 To store (n) samples, use the key sequence <n> SHIFT STORE (n) where <n> is a valid integer. To recall (n) samples for display, use the key sequence SHIFT RECALL (n). Pushing RESET restarts the period of (n) samples.

3.4.7.3 High/Low Values

3.4.7.3.1 Use Special Function 51 and key sequences 51 SHIFT STORE SF and SHIFT SF to calculate and display the High value of (n) samples. Use Special Function 52 and key sequences 52 SHIFT STORE SF and SHIFT SF to calculate and display the Low value of (n) samples. If enabled, the MEAN(n) or STD(n) key is disabled during determination of High/Low values.

3.4.7.4 MEAN(n)/STD(n) Functions

3.4.7.4.1 Successively use key sequence SHIFT MEAN(n) or SHIFT STD(n) to enable and disable the corresponding statistical function. Pressing SHIFT MEAN(n)/SHIFT STD(n) automatically deselects the opposite function if enabled. Updating of the main display for either statistical function only occurs after (n) samples have been executed.

3.4.8 Special Functions

3.4.8.1 Table 3.14 lists the special functions available on the 1995/1996. All special functions are designated by either a two or three-digit special function number (NN or NN.N). In the table, special functions are organized by mutually exclusive groups shown by lined sections. Selecting a member of one of these groups automatically deselects all other special functions in that group. Storing a circled special function disables all special functions in a group. Circled special functions may not be recalled.

3.4.8.2 Special Function Storage

3.4.8.2.1 Special function numbers must be entered into memory before special functions can be enabled. Use the following key sequence to store, for example, special function number 81: 81 SHIFT STORE SF.

3.4.8.2.2 The digits for a special function number are shown on the main display as the numeric keys are pressed. Once the number is stored, the counter automatically returns to the measurement mode. Storing a special function number overwrites other numbers within its group.

3.4.8.3 Special Function Recall

3.4.8.3.1 Stored special functions are recalled to the main display using key sequence SHIFT RECALL SF. The lowest special function number in memory will be shown first on the display. Use the RESOLUTION keys (↑↓) to scroll through the current set of special function numbers.

3.4.8.4 Special Function Enabling/Disabling

3.4.8.4.1 Enable and disable stored special functions by successively using key sequence SHIFT SF. The LED lights when special functions are enabled.

NOTE:

Storing a special function when special functions are enabled immediately enables that special function.

Table 3.14 - Special Functions (SFs)

SF Number	Function
0	No special functions. Storing SF0 erases all current special functions. SF0 r be recalled for display. SF0 is present after power-up
20	Default for SF 21. Normal Inputs A and B
21	Inputs A and B exchanged
27	Default for SFs 28, 29. Filter functions for both Inputs A and B
28	Filter key functions with Input A only
29	Filter key functions with Input B only
30	Default for SF 31. Continuous Auto-Trigger mode
31	Single-Shot Auto-Trigger mode
40	Default for SF 41. Read rate of 300 ms
41	Maximum read rate
50	Default for SFS 51, 52. Normal statistics operation
51	Display highest value for (n) samples
52	Display lowest value for (n) samples
60	Default for SF 61. Automatic start/stop totalize
61	Manual start/stop totalize
70	Keypad test for front-panel LEDs. No SF enabling necessary; just store the SF to initiate the test
80	Default for SFs 80 - 90. No external arming, external gate, or synchrc window auto-trigger (Syn. Wind. AT)

Table 3.14 – Special Functions (Cont'd)

SF Number	Function	
81	External arming off	
82.0	Ext. arming, (+) slope	- Input A
82.1	↓	- Input B
82.2		- Input D, Zero-Crossing Trigger Level
82.3		- Input D, TTL-Crossing Trigger Level
	(82.3 is the default for SFs 82.0 - 82.3)	
83.0	Ext. arming, (–) slope	- Input A
83.1	↓	- Input B
83.2		- Input D, Zero-Crossing Trigger Level
83.3		- Input D, TTL-Crossing Trigger Level
	(83.3 is the default for SFs 83.0 - 83.3)	
84	External gate off	
85.0	Ext. gate, start (+) stop (+)	- Input A
85.1	↓	- Input B
85.2		- Input D, Zero-Crossing Trigger Levels
85.3		- Input D, TTL-Crossing Trigger Levels
	(85.3 is the default for SFs 85.0 - 85.3)	
86.0	Ext. gate, start (+) stop (–)	- Input A
86.1	↓	- Input B
86.2		- Input D, Zero-Crossing Trigger Levels
86.3		- Input D, TTL-Crossing Trigger Levels
	(86.3 is the default for SFs 86.0 - 86.3)	
87.0	Ext. gate, start (–) stop (+)	- Input A
87.1	↓	- Input B
87.2		- Input D, Zero-Crossing Trigger Levels
87.3		- Input D, TTL-Crossing Trigger Levels
	(87.3 is the default for SFs 87.0 - 87.3)	
88.0	Ext. gate, start (–) stop (–)	- Input A
88.1	↓	- Input B
88.2		- Input D, Zero-Crossing Trigger Levels
88.3		- Input D, TTL-Crossing Trigger Levels
	(88.3 is the default for SFs 88.0 - 88.3)	
90	Synchronous Window Auto-Trigger (Syn. Wind. AT) off	
91.0	Syn. Wind. AT, start (+) stop (+)	- Input A
91.1	↓	- Input B
91.2		- Input D, Zero-Crossing Trigger Levels
91.3		- Input D, TTL-Crossing Trigger Levels
	(91.3 is the default for SFs 91.0 - 91.3)	
92.0	Syn. Wind. AT, start (+) stop (–)	- Input A
92.1	↓	- Input B
92.2		- Input D, Zero-Crossing Trigger Levels
92.3		- Input D, TTL-Crossing Trigger Levels
	(92.3 is the default for SFs 92.0 - 92.3)	

Table 3.14 - Special Functions (Cont'd)

SF Number	Function	
93.0	Syn. Wind. AT, start (-) stop (+)	- Input A
93.1		- Input B
93.2		- Input D, Zero-Crossing Trigger L
93.3		- Input D, TTL-Crossing Trigger L
	(93.3 is the default for SFs 93.0 - 93.3)	
94.0	Syn. Wind. AT, start (-) stop (-)	- Input A
94.1		- Input B
94.2		- Input D, Zero-Crossing Trigger L
94.3		- Input D, TTL-Crossing Trigger L
	(94.3 is the default for SFs 94.0 - 94.3)	

NOTE:

When the main function of the 1995/1996 is changed, Special Functions 80 - 94 are reviewed. If setup conditions are appropriate for the new function, they are retained; if they are not, they are cancelled. The setup conditions, however, are reactivated when the original function is reselected because of the counter's one level of keyboard memory.

3.4.9 Error Codes

3.4.9.1 Table 3.15 lists the error codes that may be displayed by the counter during local operation either as "OP Error" or in the form "Error NN" where NN is a 2-digit code number. Error codes will clear automatically after displaying for about 2-3 seconds.

Table 3.15 - Error Codes

Displayed Codes	Error
OP Error	Key invalid in present machine state or key out-of-sequence
Error 20	Input number out-of-range
23	Phase measurement ratio out-of-range
24	Hardware ratio measurement ratio produced divide by zero
25	Internal totalize error
34	Display underflow
35	Display overflow
40	Non-Vol Memory error during calibration
41	Non-Vol Memory error-data verification failure of machine setup store
42	Non-Vol Memory error-attempted recall of nonexistent machine setup store
50	Normalize function error (R-X)Y/Z
51	Statistical calculation error
60	Internal self-test: RAM
61	Internal self-test: ROM
62	Internal self-test: Non-Vol Memory
63	Internal self-test: measurement amplifier failure

Table 3.15 - Error Codes Cont'd)

Displayed Codes	Error
64	Internal self-test: measurement logic failure
70	Floating point addition error
71	Floating point multiplication error
72	Floating point division error
73	Floating point compare error
74	Floating point operation undefined
75	Floating point underflow
76	Floating point overflow
78	ASCII to floating point conversion error
79	Floating point to ASCII conversion error
80	Double precision compare error
81	Double precision to ASCII error
82	Double precision to floating point conversion error
83	Integer division by zero
99	Internal software error

Table 3.16 - Non-Vol Memory Locations

Function/Description	Location
Non-vol memory recall from 0-9 Non-vol memory store from 0-9	0-9 0-9 (see Notes)

NOTE 1:

Storing a setup (memory locations 0-9) requires a nominal 2-second wait after keyboard entry.

NOTE 2:

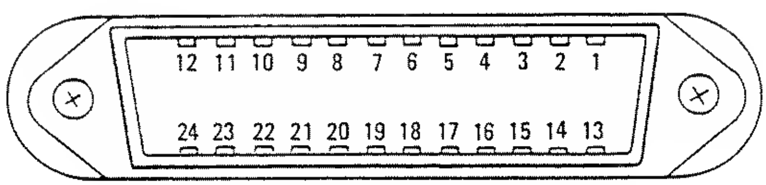
Calibration constants can only be viewed when the unit is in the Check mode. Also, calibration constants are only stored during the CAL Store step of the calibration procedure (see Section 6).

Function/Description	Location
Recall calibration constants:	
DAC constants	
Input A slope multiplier	10
Input A slope offset	11
Input B slope multiplier	12
Input B slope offset	13
Input path constants	
Input A start, hyst. low, offset	14
Input A start, hyst. low, hysteresis	15
Input A start, hyst. high, offset	16
Input A start, hyst. high, hysteresis	17
Input A stop, hyst. low, offset	18
Input A stop, hyst. low, hysteresis	19
Input A stop, hyst. high, offset	20
Input A stop, hyst. high, hysteresis	21
Input B start, hyst. low, offset	22
Input B start, hyst. low, hysteresis	23
Input B start, hyst. high, offset	24
Input B start, hyst. high, hysteresis	25
Input B stop, hyst. low, offset	26
Input B stop, hyst. low, hysteresis	27
Input B stop, hyst. high, offset	28
Input B stop, hyst. high, hysteresis	29
Time Interval constants	
A-start, B-stop; A-positive, B-negative	30
A-start, A-stop; A-negative, B-positive	31
B-start, A-stop; A-positive, B-negative	32
B-start, B-stop; A-negative, B-positive	33

4.1 GENERAL PURPOSE INTERFACE BUS (GPIB)

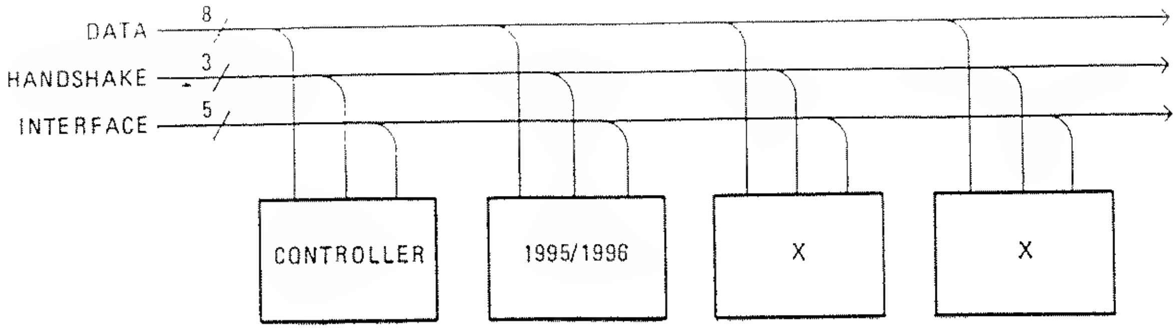
4.1.1 Introduction

4.1.1.1 This subsection provides operating information for the 1995/1996 using the GPIB system interface. The IEEE-488-1978 interface permits remote control of all the counter's functions except POWER ON/OFF. Inputs and outputs are made via a standard 24-pin GPIB connector (see Figure 4.1) on the rear panel. Pin location, signal line identification, and GPIB operation comply with IEEE-STD-488-1978. The GPIB provides interface capability with other instruments and a controller also using the interface-bus structure (see Figure 4.2). This figure also shows signal line designations and pin assignments. IEEE-STD-488-1978 subsets available are listed in Table 4.1.



Pin No.	Assignment	Pin No.	Assignment
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND, (6)
7	NRFD	19	GND, (7)
8	NDAC	20	GND, (8)
9	IFC	21	GND, (9)
10	SRQ	22	GND, (10)
11	ATN	23	GND, (11)
12	SHIELD	24	GND, (5 and 17)

Figure 4.1 - GPIB Connector (Rear Panel)



Pin	Nomenclature	Description
1 2 3 4 13 14 15 16	DIO-1 Data In/Out Bit 1 (LSB) DIO-2 Data In/Out Bit 2 DIO-3 Data In/Out Bit 3 DIO-4 Data In/Out Bit 4 DIO-5 Data In/Out Bit 5 DIO-6 Data In/Out Bit 6 DIO-7 Data In/Out Bit 7 DIO-8 Data In/Out Bit 8	Data lines are used to transfer data from one instrument to another
6 7 8	DAV (Data Valid) NRFD (Not Ready for Data) NDAC (Not Data Accepted)	Handshake lines operate in a proper time sequence for complete communication between instruments
5 9 10 11 17	EOI (End or Identify) IFC (Interface Clear) SRQ (Service Request) ATN (Attention) REN (Remote Enable)	Interface lines are used to provide an orderly flow of information between units
12 18 19 20 21 22 23 24	SHIELD GND (6) GND (7) GND (8) GND (9) GND (10) GND (11) GND (5 and 17)	

Figure 4.2 - Interface Signal Pin Assignments

4.2 GPIB DESCRIPTION

4.2.1 Refer to Figure 4.2. There are 24 lines available at the GPIB connector, including 16 signal and 7 ground return lines, and one shield. All of the data bus lines are either input or output lines, having the following characteristics:

Logic Levels:	1 = Low = $\leq .8V$
	0 = High = $\geq 2.0V$
Input Loading:	Each input = one TTL load
Output:	The output is capable of driving 15 interface bus loads. It consists of an open-collector driver and is capable of sinking 48 mA with a maximum voltage drop of 0.5 volts. See the IEEE-488 Electrical Specifications.

Table 4.1 - IEEE-488-1978 Standard Interface Subset Capability

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T5	Talker	Complete Capability (1) Basic Talker (2) Serial Poll (3) Talk Only Mode (4) Unaddress if MLA
TE0	Extended Talker	None
L4	Listener	Complete except Listen Only (1) Basic Listener (2) Unaddress if MTA
LE0	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability (1) REN - Remote Enable (2) LLO - Local Lockout (3) GTL - Go to Local
PP0	Parallel Poll	No Capability
DC1	Device Clear	Complete Capability (1) DCL - Device Clear (2) SDC - Selected Device Clear
DT1	Device Trigger	Complete Capability GET - Group Execute Trigger
C0	Controller	No Capability
E1	Open Collector Bus Drivers	

4.2.2 The signal lines shown in Figure 4.2 consist of three functionally separate sets: Data, Handshake, and Interface.

4.2.2.1 Data - the data lines consist of DIO-1 to DIO-8. These lines are the signal channels over which data flows between all instruments on the bus in bit-parallel, byte-serial form.

4.2.2.2 Handshake - these three transfer lines consist of: DAV (Data Valid), NDAC (Not Data Accepted), and NRFD (Not Ready for Data). These lines provide communication between GPIB bus members (i.e., between the instrument that is talking and the instrument(s) that are listening) to synchronize the information flow across the eight data lines. These lines derive their nomenclature from their meaning in the low or 1 state (e.g., when NRFD is low, the device is Not Ready for Data).

a. DAV - signifies that valid information is available on the data lines

b. NRFD - signifies that the instrument is not ready to accept information

c. NDAC - signifies that information is not accepted by the acceptor bus device

4.2.2.3 Interface - these five interface lines coordinate the information flow on the bus.

a. IFC (Interface Clear) - places the instrument in the Idle state (i.e., Untalk, Unlisten)

b. ATN (Attention) - indicates the kind of information on the data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data

c. REN (Remote Enable) - arms the instrument to select Remote operation when it's addressed as a listener

d. SRQ (Service Request) - signals the system controller that a peripheral device or bus member wants attention for purposes such as transmitting measurement, status, or condition information to the system controller

e. EOI (End or Identify) - used for (1) signifying the end of a message and (2) signalling bus peripherals to set the I/O bit assigned for parallel poll identification

4.2.3 GPIB Handshake

4.2.3.1 The handshake sequence is the process by which each data byte is transferred from the source to the acceptor.

4.2.3.2 Refer to Figure 4.3. It shows the sequential relationship between the DAV, NFRD, and NDAC lines used to transfer data bytes. Figure 4.4 shows the handshake flow chart.

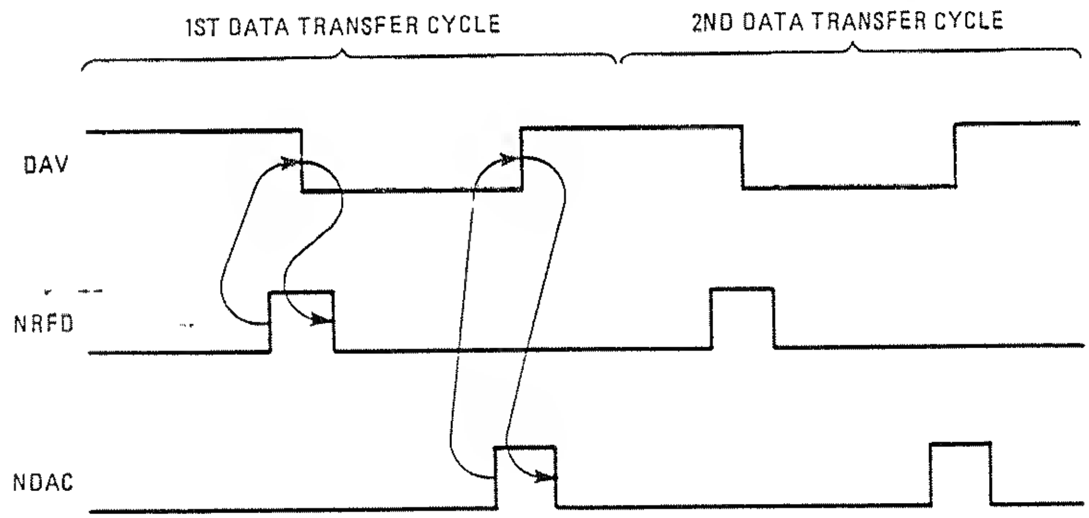


Figure 4.3 - Handshake Sequence

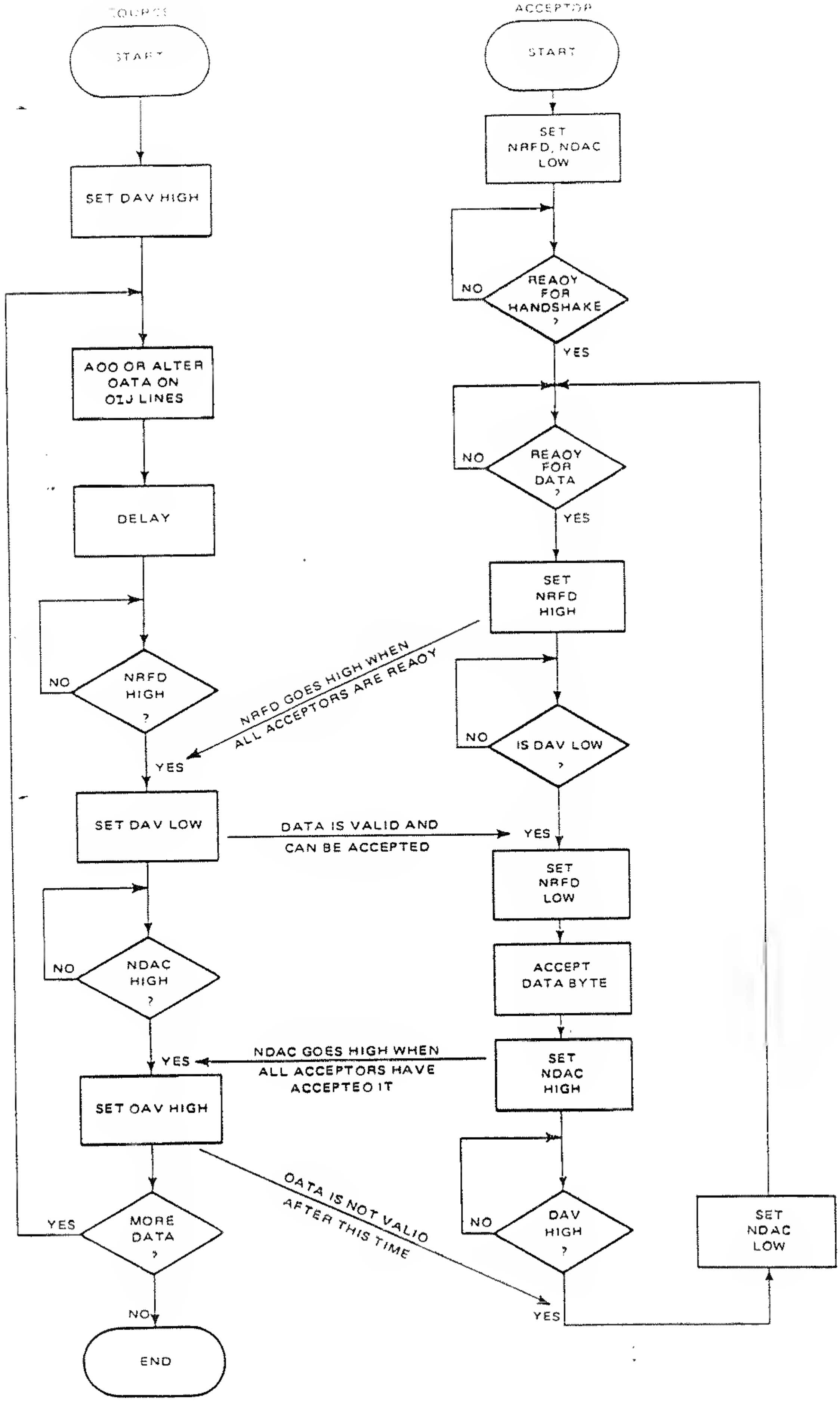


Figure 4.4 – Handshake Flow Chart

4.3 GPIB ADDRESS ASSIGNMENT

4.3.1 The 1995/1996 must be assigned an address as a bus member when operating in a GPIB system. Assigning an address to the counter permits it to be "called up" by the system controller or other resident bus device without interfering with it.

4.3.2 Table 4.2 provides the available numbers for programming the counter's GPIB address and determining the various talk/listen address codes used in programming the controller.

4.3.3 To program the counter's address, use key sequence <number> SHIFT STORE ADDR where <number> is any number from 00 through 30. To recall the counter's address, use key sequence SHIFT RECALL ADDR. To change the counter's address, simply enter the new address. The new GPIB address will overwrite the old one. The counter will automatically return to its measurement mode.

4.3.4 To enable the Talk-Only mode, just enter 99 as the new address. This will not affect the counter's selected bus address (00 through 30), but will set the unit to respond only as a talker (see Subsection 4.5.2 for details). To exit the Talk-Only mode, just reenter the counter's selected bus address or a new bus address.

NOTE:

Printed instructions for address programming are found on the rear panel just to the right of the GPIB connector.

4.3.5 Observe in the table that the far right column lists the number addresses that can be assigned to the counter. Once an address has been selected and stored, the controller may then address the 1995/1996 as a talker/listener by transmitting the appropriate ASCII character on the data lines. The "DATA LINES" column of the table shows the 7-bit binary codes for every talk/listen address assigned to the counter. The controller transmits these codes to the counter to establish its talker/listener status.

4.3.6 Note also in the table that there are two address codes for each GPIB address number. Each code represents a different ASCII character. For example, if an address of 02 is assigned to the counter, the talk address is ASCII character B and the listen address is ASCII character ". The only difference in the binary code in each case is the state of data lines D6 and D7.

4.3.7 The counter is preset at GPIB address 03 when shipped.

Table 4.2 - 1995/1996 GPIB Address and Talk/Listen Codes

ASCII CHARACTERS		DATA LINES							DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	
				ADDRESS					
TALK	LISTEN	TALK	LISTEN	16	8	4	2	1	
	SP	0	1	0	0	0	0	0	00
@		1	0	0	0	0	0	0	
	!	0	1	0	0	0	0	1	01
A		1	0	0	0	0	0	1	
	"	0	1	0	0	0	1	0	02
B		1	0	0	0	0	1	0	
	#	0	1	0	0	0	1	1	03
C		1	0	0	0	0	1	1	
	$	0	1	0	0	1	0	0	04
D		1	0	0	0	1	0	0	
	%	0	1	0	0	1	0	1	05
E		1	0	0	0	1	0	1	
	&	0	1	0	0	1	1	0	06
F		1	0	0	0	1	1	0	
	' (APOSTROPHE)	0	1	0	0	1	1	1	07
G		1	0	0	0	1	1	1	
	(	0	1	0	1	0	0	0	08
H		1	0	0	1	0	0	0	
	)	0	1	0	1	0	0	1	09
I		1	0	0	1	0	0	1	
	•	0	1	0	1	0	1	0	10
J		1	0	0	1	0	1	0	
	+	0	1	0	1	0	1	1	11
K		1	0	0	1	0	1	1	
	,	0	1	0	1	1	0	0	12
L		1	0	0	1	1	0	0	
	–	0	1	0	1	1	0	1	13
M		1	0	0	1	1	0	1	
	.	0	1	0	1	1	1	0	14
N		1.	0	0	1	1	1	0	
	/	0	1	0	1	1	1	1	15
C		1	0	0	1	1	1	1	

Table 4.2 - 1995/1996 GPIB Address and Talk/Listen Codes (Cont'd)

ASCII CHARACTERS		DATA LINES							DECIMAL ADDRESS
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	
				ADDRESS					
TALK	LISTEN	TALK	LISTEN	16	8	4	2	1	
	Ø	0	1	1	0	0	0	0	16
P		1	0	1	0	0	0	0	
	1	0	1	1	0	0	0	1	17
Q		1	0	1	0	0	0	1	
	2	0	1	1	0	0	1	0	18
R		1	0	1	0	0	1	0	
	3	0	1	1	0	0	1	1	19
S		1	0	1	0	0	1	1	
	4	0	1	1	0	1	0	0	20
T		1	0	1	0	1	0	0	
	5	0	1	1	0	1	0	1	21
U		1	0	1	0	1	0	1	
	6	0	1	1	0	1	1	0	22
V		1	0	1	0	1	1	0	
	7	0	1	1	0	1	1	1	23
W		1	0	1	0	1	1	1	
	8	0	1	1	1	0	0	0	24
X		1	0	1	1	0	0	0	
	9	0	1	1	1	0	0	1	25
Y		1	0	1	1	0	0	1	
	:	0	1	1	1	0	1	0	26
Z		1	0	1	1	0	1	0	
	;	0	1	1	1	0	1	1	27
[		1	0	1	1	0	1	1	
	<	0	1	1	1	1	0	0	28
\		1	0	1	1	1	0	0	
	=	0	1	1	1	1	0	1	29
]		1	0	1	1	1	0	1	
	>	0	1	1	1	1	1	0	30
^		1	0	1	1	1	1	0	
NONE		ILLEGAL							31

4.4 INTERFACE MESSAGE REPERTOIRE and RESPONSE

4.4.1 Introduction

4.4.1.1 The 1995/1996 is equipped with a standard GPIB interface designed to meet IEEE-STD-488-1978 specifications. These specifications provide a definition of multiline interface messages, dividing them into two main groups:

a. Primary command group

b. Secondary command group

This counter includes only the primary commands in its interface repertoire.

4.4.1.2 The primary command group is further divided into four categories:

a. Listen address commands

b. Talk address commands

c. Addressed commands

d. Universal commands

4.4.2 Listen and Talk Address Commands

4.4.2.1 The counter is designed to include 31 listen and 31 talk addresses. (Table 4.2 lists these addresses.) The instrument responds to address messages as defined by the programmed GPIB address entered from the counter's front panel.

4.4.2.2 Listen Addresses

4.4.2.2.1 Receipt by the counter of a listen address makes it a listener. If previously addressed to talk, the counter ceases to be a talker. In Local mode, the counter reverts to its Remote state, provided the REN message is true.

4.4.2.3 Talk Addresses

4.4.2.3.1 Receipt by the counter of a talk address makes it a talker. If previously addressed to listen, the counter ceases to be a listener. If in Local mode, the counter will remain under local control.

4.4.2.4 Talk Addresses-Other Devices

4.4.2.4.1 If the counter was previously addressed to talk, then receives the talk address of another bus device, the 1995/1996 ceases to be a talker.

4.4.3 Addressed and Universal Commands

4.4.3.1 Table 4.3 lists the Addressed and Universal commands to which the 1995/1996 responds. These interface commands are recognized because they are sent with the ATN message as true. The following paragraphs describe the counter's response to each of these commands.

Table 4.3 - Addressed and Universal Commands

Message	Meaning	Hex Code	Decimal Equivalent	Data Line Code 7	6	5	4	3	2	1
GTL	Go To Local	01	1	0	0	0	0	0	0	1
SDC	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	20	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	95	1	0	1	1	1	1	1

4.4.3.2 Go To Local (GTL)

4.4.3.2.1 Provided the counter is in remote and a listener, it reverts to local operation. The counter remains addressed to listen. It now operates by front-panel controls, until returned to remote control by receipt of the first byte of a device-dependent message. The decimal and hex equivalents are both 01. When in local, the SRQ LED is always off.

NOTE:

If the counter is in a function having no equivalent in local operation, upon receipt of a GTL command, it will default to home state conditions. These functions include: hardware ratios B/A, A/C, B/C; totalize A or B by gate time; and totalize A or B by D.

4.4.3.3 Selected Device Clear (SDC)

4.4.3.3.1 Provided the counter is in remote and a listener, it reverts to home state. The condition of the GPIB interface remains unchanged. The decimal and hex equivalents are both 04.

4.4.3.4 - Group Execute Trigger (GET)

4.4.3.4.1 Provided the counter is a listener and no measurement is in progress, it executes a previously programmed measurement and, if the SRQ mask is set, issues an SRQ command at completion. The GET command permits several bus devices to simultaneously perform a number of different operations. (All bus members have been previously programmed to perform a function on receiving the GET command or trigger command.) The decimal and hex equivalents are both 08.

4.4.3.5 Local Lockout (LLO)

4.4.3.5.1 The counter responds to the LLO command regardless of its addressed state. The LLO command disables the LOCAL key on the front panel. By issuing a GTL command, the counter is returned to local control. However, if the counter is returned to remote operation, the local lockout condition is still active. The only way to deactivate the LLO condition is to turn off the counter.

4.4.3.6 Device Clear (DCL)

4.4.3.6.1 Same as the SDC command, except that all bus devices in remote are put in home state. The counter responds to this command regardless of its addressed state. The decimal and hex equivalents are 10 and 14, respectively.

4.4.3.7 Serial Poll Enable (SPE)

4.4.3.7.1 This command permits all bus members, including the counter, to set their SRQ line to binary 1, informing the controller that attention is required. For the 1995/1996, bit 7 of the status byte is set. Each bus member, having been made a talker, is then serially interrogated by the controller to determine which bus member(s) requested service and the purpose of each request. Bus members respond by transmitting their respective status bytes to the controller. All members respond to the SPE command regardless of their addressed state. The function and format of the 1995/1996's SRQ status byte is described in Subsection 4.7. The decimal and hex equivalents are 24 and 18, respectively.

4.4.3.8 Serial Poll Disable (SPD)

4.4.3.8.1 This command returns all bus members to normal operation after completion of a serial poll. All bus members respond to the SPD command regardless of their addressed state. If addressed to talk, a bus device will put its data output string on the GPIB, provided such data is available in its output buffer. The decimal and hex equivalents are 25 and 19, respectively.

4.4.3.9 Untalk (UNT)

4.4.3.9.1 This universal command instructs all talkers, including the counter, to return to their untalk or talker-idle state. All bus members are also removed from their talker state whenever a talk address other than their own is received. In the Untalk state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 9 and 5F, respectively.

4.4.3.10 Unlisten (UNL)

4.4.3.10.1 This universal command instructs all listeners, including the counter, to return to their unlisten or listen-idle state. In the Unlisten state, the front-panel ADDR LED is turned off. The decimal and hex equivalents are 63 and 3F, respectively.

4.5 GPIB OPERATING MODES

4.5.1 Introduction

4.5.1.1 Before operating the counter on the GPIB, ensure that the instrument has been assigned its correct bus address (see Subsection 4.3) and that the correct AC line voltage has been selected (see Subsection 2.7.3). The last instruction is especially important if the 1995/1996 is being used for the first time or at a new location.

4.5.1.2 The 1995/1996 can be operated on the GPIB in either its Talk-Only or Addressed mode.

4.5.2 Talk-Only Mode

4.5.2.1 To set the counter in this mode, enter counter address 99.

4.5.2.2 The Talk-Only mode may be used in systems not having a controller. Such a system permits remote reading of counter measurement data, however, the instrument is controlled from the front panel (see Section 3).

4.5.2.3 The counter determines the rate at which measurements are made. The output buffer is updated at the end of each measurement cycle, overwriting the previous measurement data if not transferred to the listener.

4.5.2.4 The listener triggers the transfer of data from the counter. The counter's output buffer is cleared when data transfer is completed.

4.5.2.5 Differences between the measurement rate and data transfer rate are resolved as follows:

a. If data transfer is in progress at the end of a measurement cycle, updating of the output buffer is delayed. Data transferred will correspond to the previous measurement cycle

b. If data transfer trigger occurs during a measurement cycle and the output buffer is empty, data transfer is delayed until the buffer is updated. Data transferred will then correspond to the latest measurement cycle

c. If a measurement cycle is completed before any byte from the previous cycle has been transferred to the listener, the buffer will be updated.

4.5.2.6 Measurement rate in the 1995/1996 can be controlled in the following ways:

a. The gate time can be controlled by selecting an appropriate display resolution or setting a specific gate time

b. A time interval delay can be set using the range of 200 ns to 100 s

c. The counter can be operated in the Hold mode (single-shot measurements). Readings are displayed indefinitely in Hold until the RESET key is pressed, initiating a new measurement cycle

4.5.3 Addressed Mode

4.5.3.1 In the Addressed mode, all of the counter's functions (except POWER ON/OFF) can be controlled using device-dependent commands (see Subsection 4.8.2). These commands are sent over the GPIB after the counter has been addressed to listen. Completed measurement readings and counter status information are then read back over the bus after the counter has been addressed to talk. If the counter is addressed to talk when its output buffer is empty, no data transfer will occur and bus activity will cease. Data transfer will start again after the output buffer is updated at the completion of the next measurement cycle.

4.6 OUTPUT MESSAGE FORMAT (TALKER)

4.6.1 Introduction

4.6.1.1 Refer to Tables 4.4 to 4.7 for the following:

a. Table 4.4 - Message formats for the various 1995/1996 measurements and "one-time" (recall) outputs

b. Table 4.5 - Basic 23-byte output format

c. Table 4.6 - Alpha header output codes

d. Table 4.7 - High speed data output format

4.6.1.2 Measurement units should be assumed as hertz, seconds, degrees, or a ratio, depending on commands previously sent to the counter.

NOTE:

An SRQ message is not sent by data recall from the counter's stores.

Table 4.4 - Measurement and "One-Time" Output Formats

Output	Format
Measurement Outputs (see NOTE 1)	
Reading (with/without math, statistics)	A single 23-byte output-see Table 4.5
Standard Deviation and Mean	A double 23-byte output (i.e., two numeric fields, with/without headers, separated by a comma, and terminated by a CRLF)
Mean, High, and Low	A triple 23-byte output (i.e., three numeric fields, with/without headers, separated by commas, and terminated by a CRLF)
"One-Time" (Recall) Outputs (see NOTE 2)	
Data Recall (e.g., gate time, math constants, TI delay, and calibration constants)	A single 23-byte output-see Table 4.5
A and B Trigger Levels	A double 23-byte output (i.e., two numeric fields, with/without headers, separated by a comma, and terminated by a CRLF)
A and B Trigger Peaks (V max., V min)	A double 23-byte output (i.e. two numeric fields, with/without headers, separated by a comma, and terminated by a CRLF)
Learn Mode	A 200-byte ASCII-formatted output sent and readable only by the counter
Error Message, Identification, or String	Variable number of ASCII bytes, null, CR, and LF

NOTE 1:

The statistics and math outputs will be the result of the calculation with the alpha header code of the function measurement. For special output (SO1), the first measurement will have the alpha header code of the normal measurement, and the second and third readings will have the alpha codes from Table 4.6 (e.g., "H" header for High).

NOTE 2:

"One-Time" (recalled) data commands must be entered in outputs by themselves. (Refer to Input Commands tabulated in Subsection 4.8 and identified with an asterisk(*). When data is recalled, it will be placed in the buffer only once. The output buffer will then default to the previously entered measurement only after the recalled data is read by the controller or the counter is programmed with a new command. Recalled data will not generate an SRQ command.

Table 4.5 - Basic 23-Byte Output Format

Byte No.	Interpretation	Permitted ASCII Characters	Notes
1	Space		Spaces are transmitted
2	Alpha header code (See Table 4.6). If turned off using the HD0 command, this byte will be a space		
3	Space		
4	Measurement Sign	+ or -	
5	Most significant digit	0 to 9	Bytes 5 to 19 will always include 14 digits (i.e., the mantissa) and decimal point. The numeric field (bytes 4 to 23) is in scientific notation. Zero's are added as necessary in the less significant digit positions.
6	Digit	0 to 9 or .	
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20	Exponent indicator	E	
21	Exponent Sign	+ or -	
22	More significant digit	0 to 9	
23	Less significant digit	0 to 9	
	CR or ,		Commas are used to separate multiple numeric field outputs.
	(LF)		Used as a final output terminator. CRLF is the final output terminator in the buffer. The EOI is always given with LF. No EOI is given if high speed mode is enabled

Table 4.6 - Alpha Header Output Codes

Function/Operation	Header	Function/Operation	Header
Frequency C	F	Ratio B/A (software)	R
Frequency A	F	Ratio C/A (software)	R
Period A	S	Ratio A/B (hardware)	R
Time Interval A→B	S	Ratio B/A (hardware)	R
Time Interval A→B with delay	T	Ratio C/B (hardware)	R
Totalize A by B	T	Ratio C/A (hardware)	R
Ratio A/B (software)	R	Rise Time B	R
Ratio C/A (software)	R	Fall Time B	S
Rise Time A	S	Positive Pulse Width B	S
Fall Time A	S	Positive Pulse Width B with delay	S S
Positive Pulse Width A	S	Negative Pulse Width B	S
Positive Pulse Width A with delay	S	Negative Pulse Width B with delay	S
Negative Pulse Width A	S	Phase B rel A	P
Negative Pulse Width A with delay	S	Duty Cycle B	U
Phase A rel B	P	Slew Rate B	S
Duty Cycle A	U	Display Mean	M
Slew Rate A	S	Display High	H
Additional Functions		Display Low	L
Frequency B	F	Recall A trigger level	A
Period B	S	Recall B trigger level	B
Time Interval B→A	S	Recall Peaks-Vmax, A or B	V
Time Interval B→A with delay	S	Recall X (Offset)	X
Manual Totalize B (software)	T	Recall Y (Normalize)	Y
Manual Totalize B (software)	T	Recall Z (Scale)	Z
Totalize B by A	T	Recall Calibration Constants	C
A by D	T	Recall n value	N
B by D	T	Recall Gate Time	G
A by gate	T	Recall Delay Time	D
		Transmit Time Out	O

NOTES:

1. In general, the following Header Codes precede the listed functions:

   F-Frequency measurements
   S-Time measurements (seconds); rise/fall times; pulse width
   P-Phase measurements
   R-Ratio measurements
   U-Duty Cycle measurements
   T-Totalize measurements

Table 4.7 - High Speed Data (ASCII) Output

ASCII Format	Value Range
b#0.nnnnnnnnnnnnnnnE#ddCRLF	0.1 to 0.999999999999999
b#N.nnnnnnnnnnnnnnnE#ddCRLF	1.0 to 9.99999999999999
b#NN.nnnnnnnnnnnnnnE#ddCRLF	10.0 to 99.9999999999999
b#NNN.nnnnnnnnnnnnnE#ddCRLF	100.0 to 999.999999999999
•	•
•	•
•	•
b#NNNNNNNNNNNNNNNN.E#ddCRLF	1000000000000000.0 to 9999999999999999.9
b#N.nnnnnnnnnnnnnnnE#ddCRLF	Any other number
where: b = blank space # = - or + N = digit n = the fractional part	• = decimal point E = exponent d = ten's exponent digit CR = carriage return LF = line feed

NOTE:

No SRQ requests are generated when in the high-speed mode.

4.7 SERVICE REQUEST (SRQ) AND STATUS BYTE

4.7.1 Introduction

4.7.1.1 An SRQ may be transmitted by the 1995/1996 whenever:

a. An error occurs

b. A measurement is completed

c. A timeout occurs

4.7.1.2 The seventh bit in the SRQ and status byte is set to a binary 1. One other bit, indicating the status or type of service requested, is also set. If an SRQ is not enabled, this other bit is still set - even if the seventh bit is not. Refer to Table 4.8 which shows the format for the counter's status byte. The front-panel SRQ LED lights when the SRQ is asserted.

Table 4.8 - Status Byte Format

Bit No.	Bit Weight	Function
1 (LSB)	1	Unused
2*	2	1 = External frequency reference in use; no SRQ issued
3	4	Unused
4**	8	1 = Timeout has occurred
5*	16	1 = Reading ready; no SRQ issued for recalled data; bit is cleared when measurement is output or when buffer is flushed
6**	32	1 = Error condition exists
7--	64	1 = Service requested
8	128	Unused

* = Serial poll alone will not clear this bit
** = Serial poll alone will clear this bit

NOTE:

Controllers vary as to positional designation of status-byte bits. Bytes are indexed in two ways: 1 through 8 with bit 1 having a weight of 1 and bit 8 having a weight of 128 (as for the 1995/1996) or 0 through 7 with bit 0 having a weight of 1 and bit 7 having a weight of 128.

4.7.1.3 The counter's SRQ status byte can be conveniently masked to indicate the type of information. This feature is achieved using the Service Request Mask command (QMn) where the value of n is the loaded bit weight (i.e., binary value) - see Table 4.8 - in the range of 0 to 255.

EXAMPLE:

If the user wants an SRQ message when (1) a timeout has occurred, and (2) an error condition exists, the correct SRQ Mask command that would generate this would be QM40 (8 + 32). Then by reading the SRQ status byte, bits 4 and 6 can be tested to determine which one caused the SRQ message.

4.7.1.4 The Service Request Mask command QM0 will disable all SRQ messages.

4.8 INPUT COMMANDS (LISTENER)

4.8.1 Introduction

4.8.1.1 The 1995/1996 responds to device-dependent commands in a "deferred" manner. This means that the GPIB interface continues to accept commands until the terminating character (LF) is received, then the entire string is executed. There is no "immediate" mode in which commands are obeyed as they are received.

4.8.1.2 The counter clears all data in its output buffer upon receiving a device-dependent command. Recalled data and single measurements, therefore, should be read immediately after the command is sent to program the counter.

4.8.2 Device-Dependent Commands

4.8.2.1 When the counter is addressed to listen, it can be controlled (except POWER ON/OFF) by device-dependent commands. These commands are tabulated below:

a. Table 4.10 - Counter Initialize Code
b. Table 4.12-Measurement Function Codes
c. Table 4.15-Math Codes
d. Table 4.16-Memory Codes
e. Table 4.17-Statistics Codes
f. Table 4.18-Gate/Delay Codes
g. Table 4.19 - Input Control Codes
h. Table 4.20 - Arming Codes
i. Table 4.21 - Learn Codes
j. Table 4.22 - Measurement Mode Codes
k. Table 4.23 - Miscellaneous Codes
l. Table 4.24 - Calibration Codes

4.8.2.2 In general, device-dependent commands are executed sequentially beginning with the first one sent, and ending with the last. However, to ensure expected results, it is recommended that the following commands be sent in a separate string: IN (Initialize), RE (Start New Measurement), SMn (Non-Vol Store to Memory, 0-9), and TG1, TG2, TG3 (Output Trigger/Peak Levels).

4.8.2.3 If more than one command is to be sent, no delimiters are required. If necessary, commas, spaces, and semicolons may be included as delimiters in the command strings for clarification without affecting counter operation. Alpha characters in a command string may be upper or lower case. Each command string must be followed by an end-of-string terminator group. Table 4.9 summarizes the valid terminator groups.

Table 4.9 – Valid Terminators

1	2	3
LF	CRLF EOI True	CRLF

NOTE:

Data output terminators are
CRLF
EOI True
in both standard and high-speed
data output modes

4.8.2.4 Table 4.10 provides the counter initialize code for the 1995/1996.

Table 4.10 – Counter Initialize Code

Function	Code
Initializes counter functions/settings to home state	IN

4.8.2.5 Some of the device-dependent commands in the following tables require additional numerical input data. Such numerical input succeeds its command. "One-time" (recall) outputs are noted by an asterisk(*). Finally, home-state commands (at power-on, after an IN command, or after a diagnostic IST command) are underlined. Refer to Table 4.11 as required for the numerical input format.

Table 4.11 - Numerical Input Format

Byte No.	Interpretation	Permitted ASCII Characteristics
1	Mantissa	+ or -
2	Most significant digit	0 to 9
3	Digit	
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17	Least significant digit	
18	Exponent indicator	E
19	Exponent sign	+ or -
20	Digit	0 to 9
21	Digit	0 to 9

NOTE 1:

The valid syntax for the numerical input value tabulated above is:

[+ or -] <H digits> [.] <I digits> [E [+ or -] <1 or 2 digits>]
where 1<= H + I<= 16. Characters inside the brackets are optional.

This format is valid for all numerical inputs including measurement functions (e.g., FN10=FN1E1). For enable/disable (i.e., toggle) commands (e.g., CK0/CK1 command), zero (CK0) will turn the command off; and any other valid numerie input (CK+1, CK55.09e-7) will turn the command on.

NOTE 2:

The use of a floating point decimal increases the number of characters in the string from 16 to 17.

NOTE 3:

Leading zeros in the mantissa and/or the exponent are ignored.

NOTE 4:

Byte one may be omitted and a positive mantissa assumed.

NOTE 5:

Bytes 2 to 17 may have up to 16 significant digits and a decimal point. The decimal point is not essential. After entry of 16 digits (without a decimal point), additional digits are ignored and a GPIB programming error is generated. Non-significant zeros will still increase the power-of-ten stored. Also, if fewer than 16 digits are required, unused bytes may by omitted.

NOTE 6:

Spaces or nulls are always ignored.

NOTE 7:

Bytes 18 to 21 (exponent group) may be omitted. Also, byte 19 may be omitted or transmitted as a space (a positive exponent should be assumed in either case).

NOTE 8:

Numbers may be terminated by one of the same terminators used for output messages, or by another device-dependent message.

NOTE 9:

Units are implied; volts for trigger levels, seconds for gate/delay times.

4.8.2.6 Table 4.12 presents the measurement function codes for the 1995/1996. Functions FN1 through FN18 are front-panel selections. Functions FN19 through FN45 are selected either as front-panel special functions or are unavailable from the keyboard. When the controller programs one of the functions (FN1-FN45), external arming, external gating, and synchronized window auto-trigger (SWAT) are turned off if invalid for the new function. If an invalid channel is programmed for a function, the command is ignored and arming, gating, or SWAT default to the off condition. No error is generated for this type of programming.

Table 4.12 - Measurement Function Codes

Function	Code
Frequency C	FN1
Frequency A	FN2
Period A	FN3
Time Interval A B	FN4
Time Interval A B with delay	FN5
Totalize A by B	FN6
Totalize A by B with delay	FN7
Ratio A/B (software)	FN8
Ratio C/B (software)	FN9
Rise Time A	FN10
Fall Time A	FN11
Positive Pulse Width A	FN12
Positive Pulse Width A with delay	FN13

Table 4.12 - Measurement Function Codes (Cont'd)

Function	Code
Negative Pulse Width A	FN14
Negative Pulse Width A with delay	FN15
Phase A rel B	FN16
Duty Cycle A	FN17
Slew Rate A	FN18
Frequency B	FN19
Period B	FN20
Time Interval B→A	FN21
Time Interval B→A with delay	FN22
Manual Totalize A	FN23
Manual Totalize B	FN24
Totalize B by A	FN25
B by A with delay	FN26
A by D (TTL)	FN27
B by D(TTL)	FN28
A by gate time	FN29
B by gate time	FN30
Ratio B/A (software)	FN31
C/A (software)	FN32
A/B (hardware)	FN33
B/A (hardware)	FN34
C/A (hardware)	FN35
C/B (hardware)	FN36
Rise Time B	FN37
Fall Time B	FN38
Positive Pulse Width B	FN39
Positive Pulse Width B with delay	FN40
Negative Pulse Width B	FN41
Negative Pulse Width B with delay	FN42
Phase B rel A	FN43
Duty Cycle B	FN44
Slew Rate B	FN45

NOTE 1:

Either "FU" or "FN" can be used for the above measurement function codes.

NOTE 2:

All measurement function codes are mutually exclusive.

NOTE 3:

For FN23 and FN24 (Manual Totalize), refer to the Gate codes to start and stop a measurement.

4.8.2.7 Table 4.13 provides the predefined (forced) setting by functions. The Phase Angle, Duty Cycle, and Slew Rate settings are automatically selected, but can be modified by the controller. In addition, for programming selection of Duty Cycle and Slew Rate settings, use the following guidelines:

a. To change from positive Duty A(B) to negative Duty A(B), program slope A(B) to minus using control code AS1

b. To change from positive Slew Rate A(B) to negative Slew Rate A(B), program slope A(B) to minus using control code AS1

NOTE:

The COMMON settings shown in the table for Phase Angle, Duty Cycle, and Slew Rate cannot be modified by the controller.

Table 4.13 - Predefined (Forced) Front-Panel Settings

Function	Common	Slope A	Slope B	DC (A and B)	Auto-Trig A	Auto-Trig
Rise Time A	On	+	+	DC	On	On
Rise Time B	On	+	+	DC	On	On
Fall Time A	On	-	-	DC	On	On
Fall Time B	On	-	-	DC	On	On
Pos. Pulse Width A	On	+	-	DC	On	On
Pos. Pulse Width B	On	-	+	DC	On	On
Neg. Pulse Width A	On	-	+	DC	On	On
Neg. Pulse Width B	On	+	-	DC	On	On
Phase A rel B	Off	+	+	DC	On	
Phase B rel A	Off	+	+	DC	On	
Duty Cycle A	On	+	-	DC	On	
Duty Cycle B	On	-	+	DC		On
Slew Rate A	On	+	+	DC	On	
Slew Rate B	On	+	+	DC		On
Man. Totalize A (software)	On					Off
Man. Totalize B (software)	On				Off	
Totalize A by Gate	On					Off
Totalize B by Gate	On				Off	
Totalize A by D	On					Off
Totalize B by D	On				Off	

NOTE 1:

When Common mode is on and the function is controlled by Input A (e.g., Frequency A, Ratio A/B), Input B autotrigger and attenuator commands are disregarded. Also in this mode, Input B levels will be ignored if Input A (and therefore B) auto-trigger is on. Similarly when the Common mode is on, and the function is controlled by Input B, Input A auto-trigger and attenuator commands are disregarded. No error is generated for this kind of inconsistent programming.

NOTE 2:

The auto-trigger must be turned off before entering a manual trigger level.

4.8.2.8 Table 4.14 indicates the valid channels for external arming and gating by function. External arming and gating are mutually exclusive commands.

Table 4.14 - Valid Channels for External Arming/Gating

Function	Valid Channels
Frequency C	A, B, D-TTL, D-Zero Crossing
Frequency A, Period A	B, D-TTL, D-Zero Crossing
Frequency B, Period B	A, D-TTL, D-Zero Crossing
Time Interval A to B†; B to A†	D-TTL, D-Zero Crossing
Totalize A by B†; B by A†	↓
Totalize A by internal gate†; B by internal gate†	↓
Rise Time A†; Rise Time B†	↓
Fall Time A†; Fall Time B†	↓
Positive Pulse Width A†; Positive Pulse Width B†	↓
Negative Pulse Width A†; Negative Pulse Width B†	↓
Slew Rate A†, Slew Rate B†	↓
Hardware Ratio A/B; Hardware Ratio B/A	↓
Hardware Ratio C/B; Hardware Ratio C/A	↓
Software Ratio A/B; Software Ratio B/A	None
Software Ratio C/B; Software Ratio C/A	↓
Duty Cycle A; Duty Cycle B	↓
Phase A rel B; Phase B rel A	↓
Totalize A by D; Totalize B by D	↓
Manual Totalize A; Manual Totalize B	↓

NOTE 1:

The dagger (†) indicates a function for which external arming is valid; external gating is invalid.

NOTE 2:

Valid channels for Synchronous Window Auto-Trig(SWAT) are identical to those for external arming/gating, except for Frequency C. SWAT is disallowed in Frequency C.

NOTE 3:

If an invalid channel is programmed for a function, the command is ignored and arming, gating, or SWAT default to the off condition. No error is generated for this type of programming.

Table 4.15 - Math Codes

Function	Code
Disable Math	MD0
Enable Math	MD1
Store Offset <value> (X)	MO <value> (home state=0)
Recall Offset	RO *
Store Normalize <value> (Y)	MN <value> (home state=1)
Recall Normalize	RN *
Store Scale <value> (Z)	MS <value> (home state=1)
Recall Scale	RS *

NOTE:

The math constant range for offset X, normalize Y, and scale Z is: ±0.000000001E-9 to ±9999999999E9.

Table 4.16 - Memory Codes

Function/Description	Code
Non-vol memory recall from 0-9 Non-vol memory store from 0-9	RM0-9 SM0-9 (see Notes)
NOTE 1: SM0-9 requires a 2-second wait after programming. **NOTE 2:** If the counter is in a function having no equivalent in local operation, this function cannot be stored in non-vol memory. These functions include: hardware ratios A/B, B/A, A/C, B/C; totalize A or B by gate time; and totalize A or B by D.	
Recall calibration constants:	
DAC constants	
Input A slope multiplier	RC10*
Input A slope offset	RC11*
Input B slope multiplier	RC12*
Input B slope offset	RC13*
Input path constants	
Input A start, hyst. low, offset	RC14*

Table 4.16 – Memory Codes (Cont'd)

Function/Description	Code
Input A start, hyst. low, hysteresis	RC15*
Input A start, hyst. high, offset	RC16*
Input A start, hyst. high, hysteresis	RC17*
Input A stop, hyst. low, offset	RC18*
Input A stop, hyst. low, hysteresis	RC19*
Input A stop, hyst. high, offset	RC20*
Input A stop, hyst. high, hysteresis	RC21*
Input B start, hyst. low, offset	RC22*
Input B start, hyst. low, hysteresis	RC23*
Input B start, hyst. high, offset	RC24*
Input B start, hyst. high, hysteresis	RC25*
Input B stop, hyst. low, offset	RC26*
Input B stop, hyst. low, hysteresis	RC27*
Input B stop, hyst. high, offset	RC28*
Input B stop, hyst. high, hysteresis	RC29*
Time Interval constants	
A-start, B-stop; A-positive, B-negative	RC30*
A-start, A-stop; A-negative, B-positive	RC31*
B-start; A-stop; A-positive, B-negative	RC32*
B-start, B-stop; A-negative, B-positive	RC33*

Table 4.17 – Statistics Codes

Function/Description	Code
Store n value = 100	SV0
Store n value = 1000	SV1
Store n value, where value = 2 to 9999	SV ⟨value⟩
Recall n value	RV *
Disable standard deviation	SD0
Enable standard deviation	SD1 – turns off mean
Disable mean	SA0
Enable mean	SA1 -turns off standard deviation
Special output disable	SO0
Special output enable	SO1 -and enable standard deviation (SD1) will output standard deviation and mean; and enable mean (SA1) will output mean, high, and low

Table 4.18 - Gate/Delay Codes

Function/Description	Code
Gate Open - used only to start software manual totalize	GO
Gate Close - used only to stop software manual totalize	GC
Gate Time Adjust - enters gate time <value> where <value>range = 200ns to 100 s; home state value = 10 ms; and a value of 0 = a single event reading	GA <value>
Recall Gate Time	RG *
Delay Time Adjust - enters delay time <value> where <value>range = 200 ns to 100 s; home state value = 1 ms	DA <value>
Recall Delay Time	RD *

4.8.2.9 To use software manual totalize (FN23 or FN24), enter the following 3 commands in order:

a. FN23 <CR LF> - sets up the manual totalize (A) function and turns on the Hold LED

b. GO <CR LF> -opens the gate to start the readings. Data can be read from the counter at this point

c. GC <CR LF> - closes the gate, turns on the Hold LED, and puts the last reading in the buffer. The last reading can be read from the counter

<u>To restart the measurement at zero enter:</u>

RE GO <CR LF>

<u>To continue the measurement count enter:</u>

GO <CR LF>

NOTE:

If a new function is entered, the single measurement mode will still be in effect.

Table 4.19 - Input Control Codes

Function/Description	Code
Trigger Level A Set	AT <value>
Trigger Level B Set - home state value is 0	BT <value>
Auto-Trig off (A and B)	AU0
Auto-Trig on (A and B)	AU1
Auto-Trig Input A off	AU2
Auto-Trig Input A on	AU3
Auto-Trig Input B off	AU4
Auto-Trig Input B on	AU5
Continuous Auto-Trig	ST0
Single Auto-Trig - use AU1, 3, or 5 to start a single autotrigger process	ST1
Coupling Input A to DC	AA0
Coupling Input A to AC	AA1
Coupling Input B to DC	BA0
Coupling Input B to AC	BA1
Slope Input A Positive	AS0
Slope Input A Negative	AS1
Slope Input B Positive	BS0
Slope Input B Negative	BS1
Attenuation Input A X 1	AX0
Attenuation Input A X 10	AX1
Attenuation Input A X 50	AX2
Attenuation Input B X 1	BX0
Attenuation Input B X 10	BX1
Attenuation Input B X 50	BX2
Impedance Input A to 1 Mohm	AZ0
Impedance Input A to 50 ohms	AZ1
Impedance Input B to 1 Mohm	BZ0
Impedance Input B to 50 ohms	BZ1
Filter Input A off	AF0
Filter Input A on	AF1
Filter Input B off	BF0
Filter Input B on	BF1
Hysteresis off	SE0
Hysteresis on	SE1
Common off (Separate mode)	CM0
Common on	CM1

Table 4.20 - Arming Codes

Function/Description	Code
External Arming Disable - internal arming enabled is home state	XA0
External Arming Input A	XA1
External Arming Input B	XA2
External Arming Input D - Zero Crossing	XA3
External Arming Input D - TTL	XA4
Arming Slope Positive	XA5
Arming Slope Negative	XA6
External Gate Disable - internal gate enabled is home state (see code GA)	XG0
External Gate Input A	XG1
External Gate Input B	XG2
External Gate Input D-Zero Crossing	XG3
External Gate Input D-TTL	XG4
Gate Slope Start-Negative; Stop-Negative	XG5
Gate Slope Start-Positive; Stop-Negative	XG6
Gate Slope Start-Negative; Stop-Positive	XG7
Gate Slope Start-Positive; Stop-Positive	XG8
Synchronous Window Auto-Trig (SWAT)	
SWAT Disable	XS0
SWAT Input A	XS1
SWAT Input B	XS2
SWAT Input D-Zero Crossing	XS3
SWAT Input D-TTL	XS4
SWAT Slope Start-Negative; Stop-Negative	XS5
SWAT Slope Start-Positive; Stop-Negative	XS6
SWAT Slope Start-Negative; Stop-Positive	XS7
SWAT Slope Start-Positive; Stop-Positive	XS8

Table 4.21 - Learn Codes

Function/Description	Code
Send Machine Setup - Learn	SL *
Receive Machine Setup - Learn	RL <total machine state string- 200 ASCII bytes>; string is readable only by the counter

Table 4.22 - Measurement Mode Codes

Function/Description	Code
Continuous Reading Mode	MM0
Single Reading Mode-use RE code to trigger a new measurement	MM1

Table 4.23 - Miscellaneous Codes

Function/Description	Code
Check Off Check On	CK0 or CH0 CK1 or CH1
Front Panel Display Disable (turns off front panel measurement display) Front Panel Display Enable	DR0 DR1
Turns Off Prefix Output Header Turns On Prefix Output Header (e.g., "F" for frequency)	HD0 HD1
High Speed Output Disable-defaults to previous autotrigger mode (single/continuous)	HS0
High Speed Output Enable-forces continuous measurement mode, turns off statistics, takes single-shot auto-trigger, and no SRQ is given. No data can be recalled at this time	HS1
Transmit Hardware Identification-that is, "RD 1995" or "RD 1996"	ID0 *
Transmit Software Identification version that is, 2.1 or other number	ID1 *
Internal Self Test-output of <space CR LF> means a successful test. Otherwise, outputs an error message. Counter returns to power-up state on exit	IST
Set SRQ Mask-where <value>=0 to 255; home state=255; and QM0 code disables all SRQ commands	QM<value>
Start New Measurement-triggers new reading in single measurement mode	RE
Program Timeout, Gate Closed home state value is 500 seconds (see Note 2)	TC<value>
Program Timeout, Gate Open where the home state value is 500 seconds; <value>=1 to 500 seconds(see Note 2)	TO<value>
Transmit Error Code-outputs <space CR LF> if no errors exist	TE *
Output Trigger Levels A and B (see Note 3)	TG1 *

Table 4.23 - Miscellaneous Codes (Cont'd)

Function/Description	Code
Output Peak Levels A (V_{max}, V_{min}) - auto-trigger A turned off (see Note 3)	TG2 *
Output Peak Levels B (V_{max}, V_{min}) - auto-trigger B turned off (see Note 3)	TG3 *
Transmit Timeout Value-total abort time is (TO + GA <value>+ TC) or if delay active (TO + DA <value> + TC), or if externally gated (TO + TC + 100 seconds)	TV *

NOTE 1:

Information for the following codes in the above table is not stored in non-vol memory: DR0, DR1; HD0, HD1; HS0, HS1; QM <value>; TC <value>,TO <value>; TV.

NOTE 2:

Program Timeout, Gate Closed refers to the time that the counter will wait for the measurement gate to close prior to issuing a timeout error. Program Timeout, Gate Open refers to the time that the counter will wait, upon receipt of trigger, for the measurement gate to open prior to issuing a timeout error.

NOTE 3:

For the TG1, TG2, and TG3 codes: if in single measurement mode (or single autotrigger mode), initiate the measurement (or trigger) first, then send the command to output trigger levels. This ensures the output of trigger levels of measurement just taken.

Table 4.24 - Calibration Codes

Function/Description		Code
NOTE 1: Each of the eight commands listed below must be on a single line. See Section 5 of this manual for the calibration procedure.		
Step 1		CAL
Step 2	Set start and stop DACs to the maximum positive voltage	CLHI
	Set start and stop DACs to the maximum negative voltage	CLLO
Step 3	Start DAC positive voltage (+X.XXXX) Stop DAC positive voltage (+X.XXXX) Start DAC negative voltage (-X.XXXX) Stop DAC negative voltage (-X.XXXX)	CLTH <Vstart-high> CLPH <Vstop-high> CLTL <Vstart-low> CLPL <VStop-low>
NOTE 2: At this point, "CAL" is shown on the main display. About five minutes later, "CAL donE" is displayed when the calibration is finished. Calibration values may now be stored to non-vol memory by holding the front-panel calibration button in and sending the CLST command.		
Step 4	Stores values to non-vol memory	CLST
NOTE 3: Upon successful completion of non-vol store, a "donE" message is displayed, a <space CR LF> GPIB output is given, and the calibration button can be released. If at any point, there is an error (e.g., syntax, calibration), the entire procedure must be repeated starting with Step 1.		

4.9 GPIB ERRORS

4.9.1 When an error occurs, an SRQ message will be generated and the SRQ LED turned on. Should multiple errors occur, only the latest error is saved. An error will be cleared and the SRQ LED turned off when the controller transmits a new command string to the counter. To read the error message, send a TE (Transmit Error) command immediately after the error occurs.

4.9.2 Table 4.25 below lists the GPIB error messages and numbered codes. The numbered error codes are in the form "Error NN" where NN is a 2-digit code.

Table 4.25 - GPIB Error Messages and Codes

Message/Code Number	Error
ALPHA SYNTAX ERROR	Alpha syntax error while parsing
NUMBER SYNTAX ERROR	Number syntax error while parsing
LEARN ERROR	Error in machine setup string from "learn"
INVALID RANGE	Range error (e.g., FN code number, gate time, delay value)
LEVEL OR ATTN INVALID	Level out-of-range for the attenuator setting
Error 23	Phase measurement ratio out-of-range
24	Hardware ratio measurement produced divide by zero
25	Internal totalize error
26	Input buffer overflow
27	Gate did not open in specified time
28	Gate did not close in specified time
29	Frequency C not permitted on Model 1995
30	Error during calibration
31	Invalid syntax during calibration parsing or commands out-of-order
32	Cannot store calibration values to Non-Vol memory-values must be entered first
33	Error during calibration store to Non-Vol memory
40	Non-Vol Memory error-the Non-Vol data did not pass verification
41	Non-Vol Memory error during recall of memory
42	Non-Vol Memory-attemped recall of nonexistent machine setup store
50	Normalize function error (R-X)Y/Z
51	Statistical calculation error
60	Internal self-test: RAM
61	Internal self-test: ROM
62	Internal self-test: Non-Vol Memory
63	Internal self-test: measurement amplifier failure
64	Internal self-test: measurement logic failure

Table 4.25 - GPIB Error Messages and Codes (Cont'd)

Message/Code Number	Error
Error 70	Floating point addition error
71	Floating point multiplication error
72	Floating point division error
73	Floating point compare error
74	Floating point operation undefined
75	Floating point underflow
76	Floating point overflow
78	ASCII to floating point conversion error
79	Floating point to ASCII conversion error
80	Double precision compare error
81	Double precision to ASCII conversion error
82	Double precision to floating point conversion error
83	Integer divison by zero
99	Internal software error

NOTE:

If an error is found in a command string, the entire string is ignored. No new programming of the counter will take place and the counter will continue taking measurements as previously set up.

5.1 INTRODUCTION

5.1.1 This section describes the general theory of operation for the Universal Systems Counters Models 1995/1996.

5.1.2 The theory of operation provided is based on the simplified overall block diagram shown in Figure 5.1. Key circuit blocks of the 1995/1996 are described and supported in this section using simplified block and schematic diagrams. These diagrams supplement the complete schematics found in Section 7 of this manual. As much as possible, the simplified schematic and block diagrams provided here are annotated with the same reference designators found in the complete schematics. This should facilitate cross-referencing between this section of the manual and the schematics.

5.1.3 Integrated circuits (ICs) in the following circuit descriptions are designated by circuit references provided on the supporting simplified block and schematic diagrams. Note that each assembly of the 1995/1996 (see Parts List, Section 8) provides a separate series of IC designations starting with U1. These designations are employed in the following key circuit descriptions. When an IC package contains more than one circuit, suffix letters are used to distinguish them (e.g., U40A). Finally, when it is necessary to identify a specific pin in an IC, the reference designator, with a suffix letter if necessary, is followed by a hyphen and then the required pin number (e.g., U40A-1).

5.2 FUNCTIONAL BLOCKS

5.2.1 The 1995/1996 counter is divided into 11 major functional blocks. Most of these blocks are located on the instrument's motherboard. The front panel block, signal conditioner block, measurement block, and channel C block are incorporated on separate board(s) which plug into the motherboard. Figure 5.1 provides an overall simplified block diagram of the 1995/1996 counter. The following is a list of these 11 functional blocks:

1. Channel A/B block (See Subsection 5.3.2)
2. Channel C block (1996 only) (See Subsection 5.3.3.)
3. Measurement logic block (See Subsection 5.3.4)
4. Display/keyboard block (See Subsection 5.3.5)
5. Microprocessor block (See Subsection 5.3.6)
6. Power supply block (See Subsection 5.3.7)
7. External arming/gating block (See Subsection 5.3.8)
8. Internal gate timer block (See Subsection 5.3.9)
9. External reference multiplier block (See Subsection 5.3.10)
10. Channel D block (See Subsection 5.3.11)
11. GPIB block (See Subsection 5.3.12)

5.2.2 - Overall Functional Operation

NOTE:

For convenience, since channels A and B are identical, only the former channel is described, unless otherwise indicated.

5.2.2.1 As one reads through the General Information and Theory of Operation sections of this manual, it might prove helpful to refer to the Overall Block Diagram found in Figure 5.1.

5.2.2.2 In general, input signals are conditioned and converted into digital information in the signal conditioning section.

5.2.2.3 The measurement section is internally configured by the microprocessor according to instructions entered via the keyboard or GPIB system. The signal to be measured and the signal from the frequency reference are fed to the measurement logic block. The measured result from here is passed to the microprocessor block. If mathematical manipulation of the result is required, this is performed by the microprocessor before the final output is passed either to the display or GPIB block.

5.2.2.4 In the digital control section, circuit timing and control signals are developed by microprocessor-based logic. This section also provides for keyboard decoding and display logic.

5.2.2.5 The interface section functions as a bidirectional port for data and control signals generated by the digital control section and the external system controller.

5.2.2.6 Overall operation of the 1995/1996 centers in two LSI chips. One chip, the MCC2 (Multiple Counter and Control Chip #2), is a combination of ECL (emitter-coupled logic) and TTL (transistor-transistor logic) circuitry. This LSI chip executes all the high-speed logic steering, gating, and counting. The second LSI chip, the MCC1 (Multiple Counter and Control Chip #1), is a CMOS device that interfaces directly with the CPU. It provides the required logic functions, counting registers for accumulating raw input data, and control lines for the MCC2 chip.

5.2.2.7 Inputs for channel A are first routed through the signal-conditioning circuitry. This circuitry performs the user-selected coupling, impedance, and attenuation operations.

5.2.2.8 After initial signal conditioning, the input measurement signal passes through a protective limiter to two parallel high-input impedance buffer/amplifier stages. These generate a differential output which is applied to a second (Schmitt) amplifier stage.

5.2.2.9 In the Schmitt amplifier stage, the measurement signal is buffered, shaped, and level-shifted. The signal output from this stage is at an ECL level and called the start signal. The start signal is then directed to the divide-by-two/multiplexing circuitry.

5.2.2.10 The multiplexer either selects the divided start signal or the start/stop signals directly. The required signal is then routed to the synchronization circuitry.

5.2.2.11 - The start signal's output from the synchronization circuitry is input to the MCC2 chip. Between the MCC2 and MCC1 chips, measurement pulses are accumulated in the event and time count registers, counted, and stored as unprocessed measurement data.

5.2.2.12 Stored raw data is then retrieved by the microprocessor, manipulated to obtain the desired measurement mode, modified as necessary by special functions, then routed to the 1995/1996's display and GPIB.

5.2.2.13 The 1995/1996 employs a special TEC (Timing Error Correction) configuration which divides the time between the reference oscillator and start/stop signals. This permits the instrument to accumulate measurement pulses to a much greater resolution. In a typical measurement, the instrument's microprocessor reads the time count and TEC registers, performs the necessary calculations, and displays the result. Between measurements, the event, time, and TEC count registers are reset while the microprocessor computes the measurement result.

5.2.2.14 Arming and gating selection for the 1995/1996 are effected through the instrument's arming/gating steering-logic circuitry. For the 1995/1996 user, arming/gating selection is much more flexible than in conventional counters. This ease-of-use results from the operator's ability to employ channel A/B inputs for selecting the various arming/gating modes. This permits input voltages as low as 25 mV at 10 MHz from the front panel. Conventional triggering levels of TTL (1.4V at 10 MHz) and zero-crossing are possible using channel D's rear-panel input.

5.2.2.15 Finally, gate-time setting for the 1995/1996 is not limited to selection by a decade-divided timebase. Rather, the counter uses an internal gate timer to select the desired gate time in a 200 ns to 100 s range. This provides resolutions of 100 ns (gate time <1 ms resolution) and .1% (gate time> 1 ms resolution).

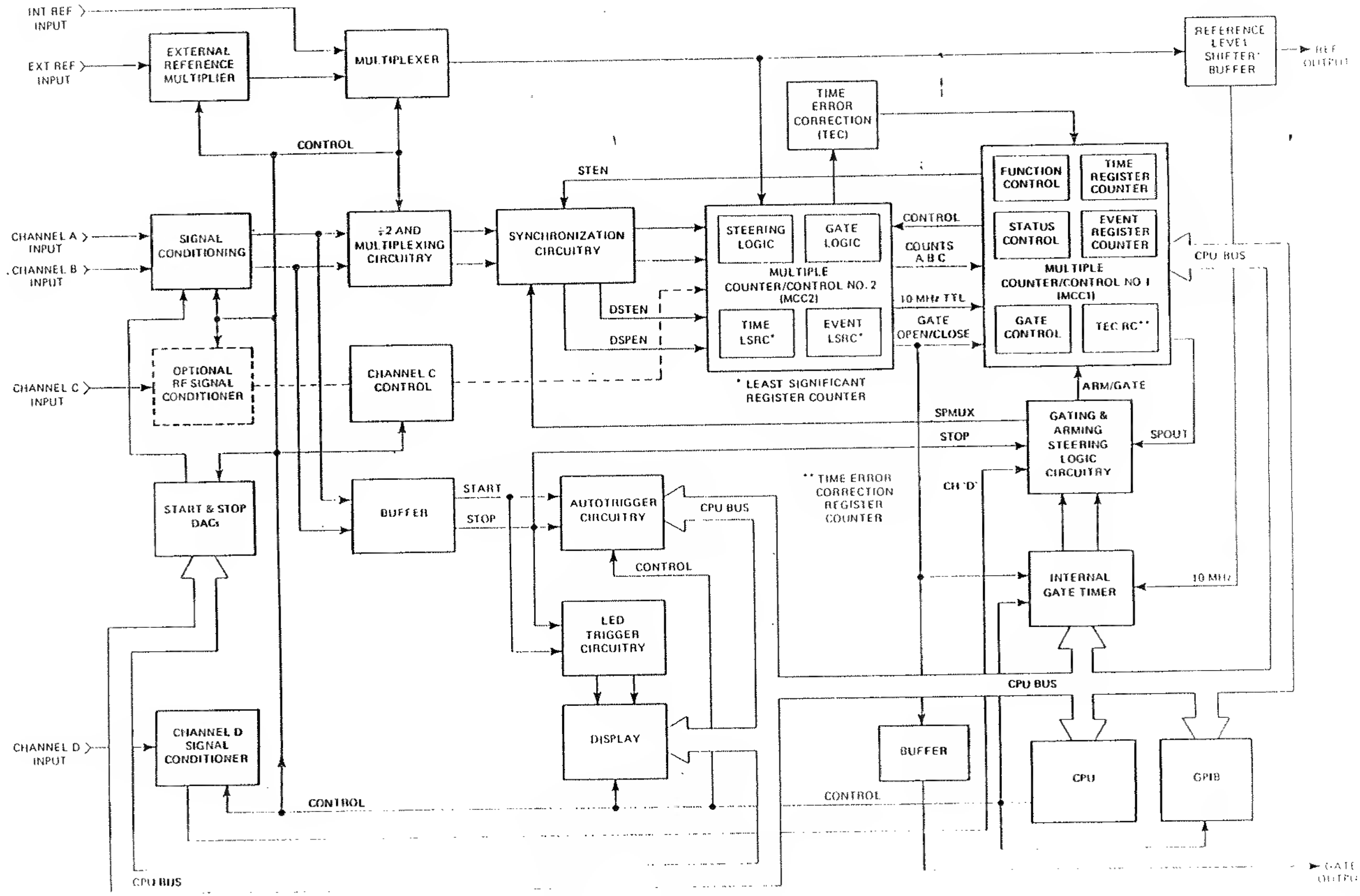


Figure 5.1 – Simplified Overall Block Diagram

5.3 - THEORY OF OPERATION BY BLOCK

5.3.1 Introduction

5.3.1.1 The 1995/1996 is divided into eleven major functional blocks. Functional and circuit theory of operation by block are described in this subsection of the manual. The figures used here are simplified schematic or block diagrams. For complete schematics, refer to Section 7.

5.3.1.2 Table 5.1 presents a list of major signal lines used in the 1995/1996 counters along with a brief functional description. Signals used together are grouped together. Included with the signal description are significant signal sources and destinations.

Table 5.1 - Signal Lines and Functions

SIGNAL NAME	SIGNAL DESCRIPTION
ARM	Arming or gating signal applied to either arm or gate a measurement
ARMSPSL	Arm stop slope select for the arming and gating circuit
ARMSTSL	Arm start slope select for the arming and gating circuit
$\overline{\text{AS}}$	Microprocessor address strobe
ATRST	Auto-trigger reset line; initializes an auto-trigger
ATSTART+	START+ signal buffered and applied to the auto-trigger circuitry
ATSTOP+	STOP+ signal buffered and applied to the auto-trigger circuitry
BW/$\overline{\text{R}}$	Microprocessor R/$\overline{\text{W}}$ inverted buffer signal (U5F)
CHANLD	Input signal applied to channel D
CHCENA	Enables channel C signal to be measured
$\overline{\text{DLYWND}}$	For future use
E	Microprocessor's enable signal for 6800-type peripherals
$\overline{\text{E}}$	Inverted microprocessor's E signal
$\overline{\text{GATE}}$	Signal that is low when the measurement gate is open
INT/$\overline{\text{EXT}}$	Selects the external reference or internal reference
LDE	Lower data enable signal generated by the microprocessor's $\overline{\text{LDS}}$ and OR-ed with the BW/$\overline{\text{R}}$ signal (U25B)

Table 5.1 - Signal Lines and Functions (Cont'd)

SIGNAL NAME	SIGNAL DESCRIPTION
$\overline{\text{LDS}}$	Microprocessor's lower data strobe
LTMS	Selects the 200 ns to 1 ms output or greater than 1 ms to 100 s output from the internal timer
$\overline{\text{LWE}}$	Lower write enable signal generated by the microprocessor's lower data strobe ($\overline{\text{LDS}}$) and OR-ed with the Read/Write (R/$\overline{\text{W}}$) signal (U24C)
MCC/$\overline{\text{GEND}}$	Selects the SPOUT or GATE END signal for ending a measurement
$\overline{\text{MLRST}}$	Main logic reset signal from the MCC1 chip
$\overline{\text{PRE}}$	Peripheral read enable signal generated by the microprocessor's R/$\overline{\text{W}}$ signal and NANDed with E signals (U4C)
$\overline{\text{RAMENA}}$	RAM enable signal, generated by the microprocessor's address strobe ($\overline{\text{AS}}$) and inverted address line A21 ($\overline{\text{A21}}$) and OR-ed together (U5C and U24A)
R/$\overline{\text{W}}$	Microprocessor's Read/$\overline{\text{Write}}$ signal
SELARM	Enables application of the ARM signal to the auto-trigger or measurement block
SELCHD	Selects the CHANLD signal as the arm or gate signal
SELSP	Selects the TTLSTOP signal as the arm or gate signal
SPMUX	Stop enable signal selection between SPOUT or $\overline{\text{GATE END}}$ signals
SPOUT	Stop enable output from MCC1 or SPEN signal
$\overline{\text{SPSL}}$	Selects the slope of the STOP+ signal
$\overline{\text{SPSLV}}$	Indicates whether the stop measurement signal is above or below the stop DAC trigger-level (TL STOP)
$\overline{\text{SPSXL}}$	Indicates that the stop measurement signal has crossed the stop DAC trigger-level (TL STOP)
START+	Input signal applied to channel A or B for selection as the START signal
STOP+	Input signal applied to channel A or B for selection as the STOP signal
$\overline{\text{STSL}}$	Selects the slope of the START+ signal

Table 5.1 - Signal Lines and Functions (Cont'd)

SIGNAL NAME	SIGNAL DESCRIPTION
$\overline{\text{STSLV}}$	Indicates whether the start measurement signal is above or below the start DAC trigger-level (TL START)
$\overline{\text{STSXL}}$	Indicates that the start measurement signal has crossed the start DAC trigger-level (TL START)
TTLSTOP	STOP+ signal converted to a TTL signal
TL START	Start channel trigger level
TL STOP	Stop channel trigger level
$\overline{\text{UDE}}$	Upper data enable signal generated by the microprocessor's $\overline{\text{LDS}}$ signal and OR-ed with the BW/$\overline{\text{R}}$ signal (U25C)
$\overline{\text{UDS}}$	Microprocessor's upper data strobe signal
$\overline{\text{UWE}}$	Upper write enable signal generated by the microprocessor's upper data strobe ($\overline{\text{UDS}}$) and OR-ed with READ/$\overline{\text{WRITE}}$ signal (R/$\overline{\text{W}}$) (U24D)
$\overline{\text{VMA+E}}$	Microprocessor's inverted enable signal ($\overline{\text{E}}$) OR-ed with the valid memory address ($\overline{\text{VMA}}$) signal (U5E and U24B)
ZERO/$\overline{\text{TTL}}$	Selects the channel D trigger point
5.20OFF	Shuts down the ECL 5.2 volts
$\overline{\text{200MHZ}}$	Enables the divide-by-two circuitry

5.3.2 Channel A/B Block

5.3.2.1 Functional Description

5.3.2.1.1 Refer to the simplified block diagram in Figure 5.2 as required. Channels A and B on the 1995/1996 are identical and only channel A is described here. Measurement signals applied to Input A are first routed through the instrument's signal conditioning circuitry. This circuitry performs selected compensation, coupling, attenuation, and impedance.

5.3.2.1.2 The measurement signal is then applied to the input of the start/stop amplifiers. The start/stop DACs (Digital-to-Analog Converters) provide a DC threshold through which the input signal must swing so that the amplifier's output will toggle.

5.3.2.1.3 The start/stop DACs have a programmable output range of ±5 VDC in increments of 2.5 mVDC. However, the trigger display only shows resolutions of 10 mVDC.

5.3.2.1.4 The signals are then routed to the start/stop output amplifiers. The switches shown in the figure permit selection of either Input A or B signal for routing to the output amplifiers. The following combinations are possible: A-start/A-stop; A-start/B-stop; B-start/B-stop; and B-start/A-stop.

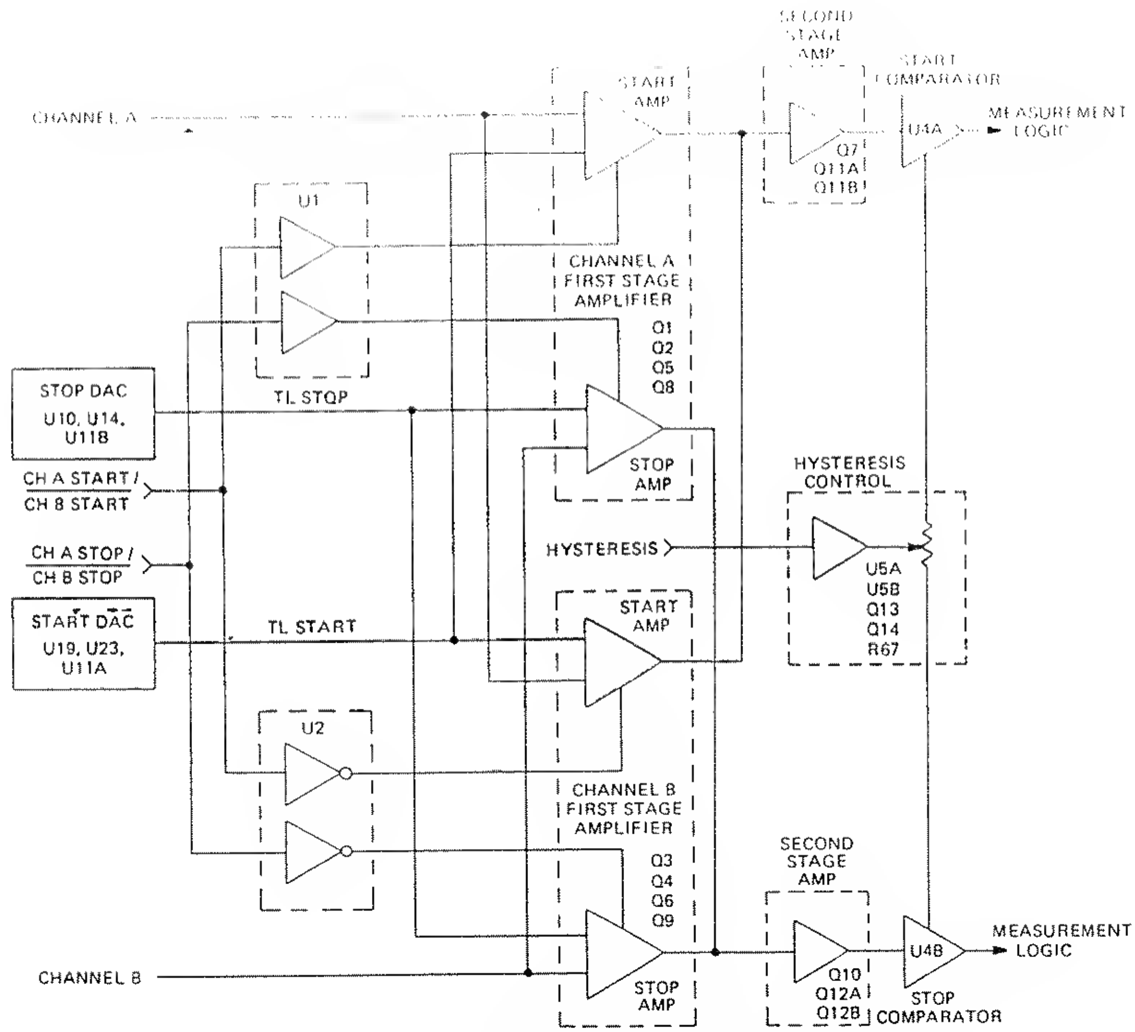


Figure 5.2 - Simplified Block Diagram for Channel A/B

5.3.2.2 **Circuit Description**

5.3.2.2.1 Input Conditioning

5.3.2.2.1.1 At the channel A input connector, K1 will select 50-ohm impedance when energized. This is achieved through the two parallel 100-ohm resistors R1 and R3. Refer to Figure 5.3.

5.3.2.2.1.2 AC/DC coupling is effected through K3. When this relay is de-energized, AC coupling is achieved via the two parallel capacitors C7 and C8.

5.3.2.2.1.3 Attenuation is accomplished via the four relays K5, K6, K10 and K12. The X1 range is set by energizing K6. When K6 is de-energized and its companion relay K5 is energized, the user will have the attenuation (X10 or X50) selected. The X10 or X50 range is selected via K12. When K12 is energized, X10 attenuation is selected. The measurement signal is attenuated by RC voltage-divider network R20, R24, C18, C22 and C32. When K12 is de-energized, X50 attenuation is achieved via RC voltage-divider network R19, R23, R82, C148, C17, C21 and C31.

5.3.2.2.1.4 When relay K9 is de-energized, the input signal is filtered by passage through R16. R16 and input capacitance work together to achieve 100 kHz nominal signal filtering.

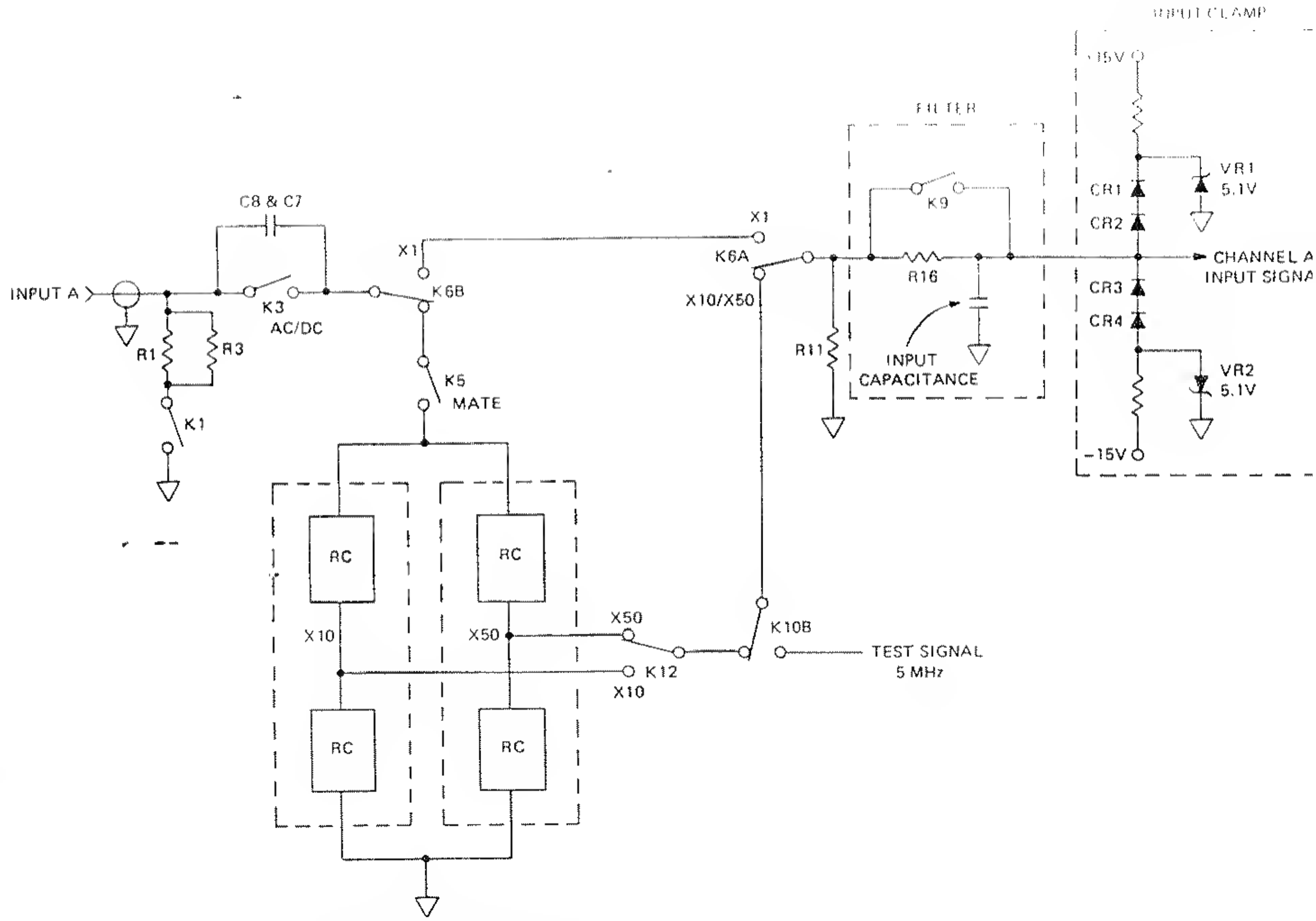


Figure 5.3 - Input Switch Circuitry for AC/DC and Attenuator

5.3.2.2.2 Start/Stop Amplifier Circuit Description

5.3.2.2.2.1 Refer to Figure 5.4. The input buffer for channel A (channel B is identical) consists of two ICs, Q8 (transistor array) and Q2 (FET array). These two chips help to comprise two differential amplifiers called the start/stop amplifiers.

5.3.2.2.2.2 Input to the start/stop amplifiers is limited to approximately ±7 volts at the input to Q2A-6 and Q2D-11. This is achieved by the input clamp circuit consisting of R31, R50, CR1, CR2, CR3, CR4, VR1, and VR2 as shown in Figure 5.3.

5.3.2.2.2.3 The current sources for these two differential stages are supplied by Q1, VR4, R32 and R33 for the start amplifier, and Q5, VR6, R36 and R37 for the stop amplifier. Each source is switched on and off by a section of U1, which in turn is controlled by a TTL-control logic signal from the motherboard.

5.3.2.2.2.4 When control line CH A START is high at U1-13, U1-11 is an open circuit. This turns on Q1 and allows current to flow. This selects the channel A input to pass through the start amplifier to the differential output (A3 and A4). If the CH A STOP control line is also high, channel A's input signal would pass through the stop amplifier to the differential output (A1 and A2). When the control line CHA START is low at U1-13, U1-11 connects the base of Q1 to -15V disabling the current source and, hence, the differential amplifier. When the amplifier is disabled, it is no longer able to process input and trigger level signals.

5.3.2.2.2.5 The amount of current through current source Q1 is determined by R32 and R33. With the HYSTERESIS control line low at U1-9 (maximum counter sensitivity), U1-2 and 16 are at -15V which puts R32 and R33 in parallel. This provides 11 mA through Q1 and 5.5 mA through each half of the differential stage. With the HYSTERESIS control line high, R32 is removed from across R33, thereby reducing the current through Q1 to 2 mA, and decreasing the counter sensitivity. Switching the current through the start and stop amplifiers, combined with hysteresis control of dual comparator U4 (Figure 5.5) controls the overall hysteresis of the signal conditioner. The amount of hysteresis determines the counter sensitivity.

5.3.2.2.2.6 The trigger levels are set by two digital-to-analog converter (DAC) circuits on the motherboard. Refer to Figure 5.6. U11A, U19, and U23 are the primary components of the START DAC; U10, U11B, and U14 (not shown) are the primary components of the STOP DAC.

5.3.2.2.2.7 The level at which the start amplifier circuit triggers is controlled by a voltage at Q2B-3 (see Figure 5.4., the TL START line). This voltage comes from U11A-1 on the motherboard as shown in Figures 5.2 and 5.6.

5.3.2.2.2.8 Thé level at which the stop amplifier circuit triggers is controlled by a voltage at Q2D-11 (see Figure 5.4, the TL STOP line). This voltage comes from U11B-8 on the motherboard as shown in Figure 5.2.

5.3.2.2.2.9 The output of the start/stop amplifiers is taken from the collector of Q8A-6 and Q8B-2 for the start and Q8C-12 and Q8D-11 for the stop amplifier. These four signals are A1, A2, A3, A4 which connect the base of Q11A, Q11B, Q12A, and Q12B as shown in Figure 5.5.

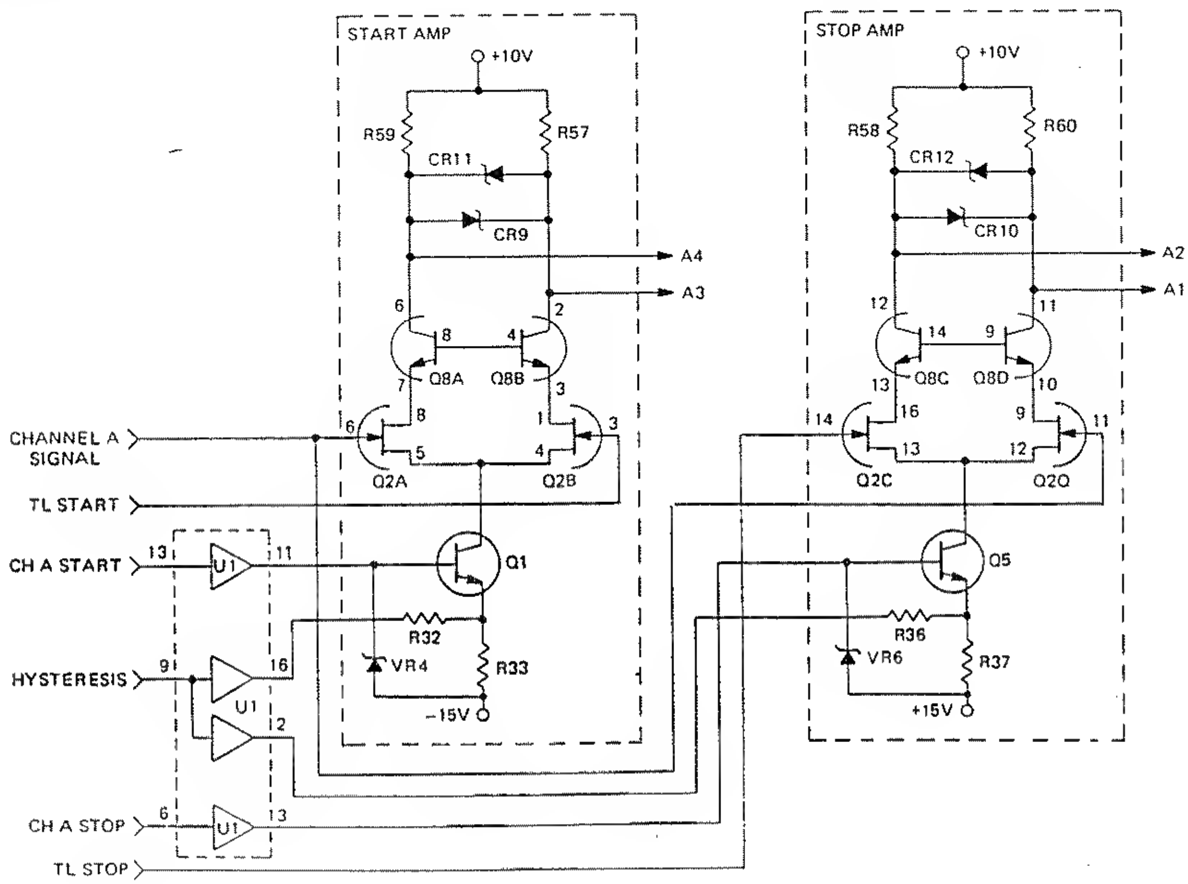


Figure 5.4 - Start/Stop Buffer Amplifier Stage

5.3.2.2.3 Start/Stop Level Shifter Circuit Description

5.3.2.2.3.1 The second amplifier stage is called the start level shifter. (For convenience, since channels A and B are identical. only channel A is discussed.) This stage is also a differential amplifier consisting of Q11A and Q11B with Q7 as the current source. Refer to Figure 5.5.

5.3.2.2.3.2 The second stage's signal is limited to a peak-to-peak swing of 400 millivolts by CR9, CR10, CR11 and CR12. These diodes improve the peak measurement accuracy of the signal conditioner at high frequencies and high input levels.

5.3.2.2.3.3 The second stage operates in the active region with a DC offset at the collector output of Q11A and Q11B. This offset is established by the current-source components Q7, R44, R51, and R52.

5.3.2.2.3.4 R44 and R52 create a voltage divider at the base of Q7, resulting in approximately 1.2 volts across R51. This, in turn, provides about 6.0 milliamps through each leg of the differential amplifier. With 6.0 milliamps through Z7-2 and Z7-3, start comparator U4A has a signal which swings around a DC offset of 200 millivolts.

5.3.2.2.4 Start/Stop Comparator Circuit Description

5.3.2.2.4.1 U4 is a dual high-speed differential comparator with an ECL output. This device receives an input from the start/stop level shifter (second amplifier stage). Refer to Figure 5.5.

5.3.2.2.4.2 U4-7 and 8 are the start differential inputs; U4-9 and 10 are the stop differential inputs. The output of the comparator is directed in two pathways: (1) measurement logic and (2) auto-trigger circuitry.

5.3.2.2.5 Hysteresis Control Circuit Description

5.3.2.2.5.1 Hysteresis control is achieved by changing the voltage applied to U4-5 and 13. This is effected by the HYSTERESIS control line which sets either a logic low or high at U5-6 in order to turn on Q13 or Q14, respectively.

5.3.2.2.5.2 With a logic low at U5-3 and 6, a high is set at the gate of Q13 and a low is set at the gate of Q14. This condition selects the low hysteresis voltage for application to U4-5 and 13 via Q13 to balancing resistor R67. This low hysteresis voltage source is established through the voltage divider network R66, R68 and R70. This voltage can be adjusted during board level calibration via variable resistors R70 and R71.

5.3.2.2.5.3 With a logic high at U5-3 and 6, Q13 is turned off and Q14 turned on. This applies the high hysteresis voltage to U4-5 and 13 via Q14 to R67. This high hysteresis voltage source is established through voltage divider network R65, R69, and R71. This voltage can be adjusted during calibration via resistor R71.

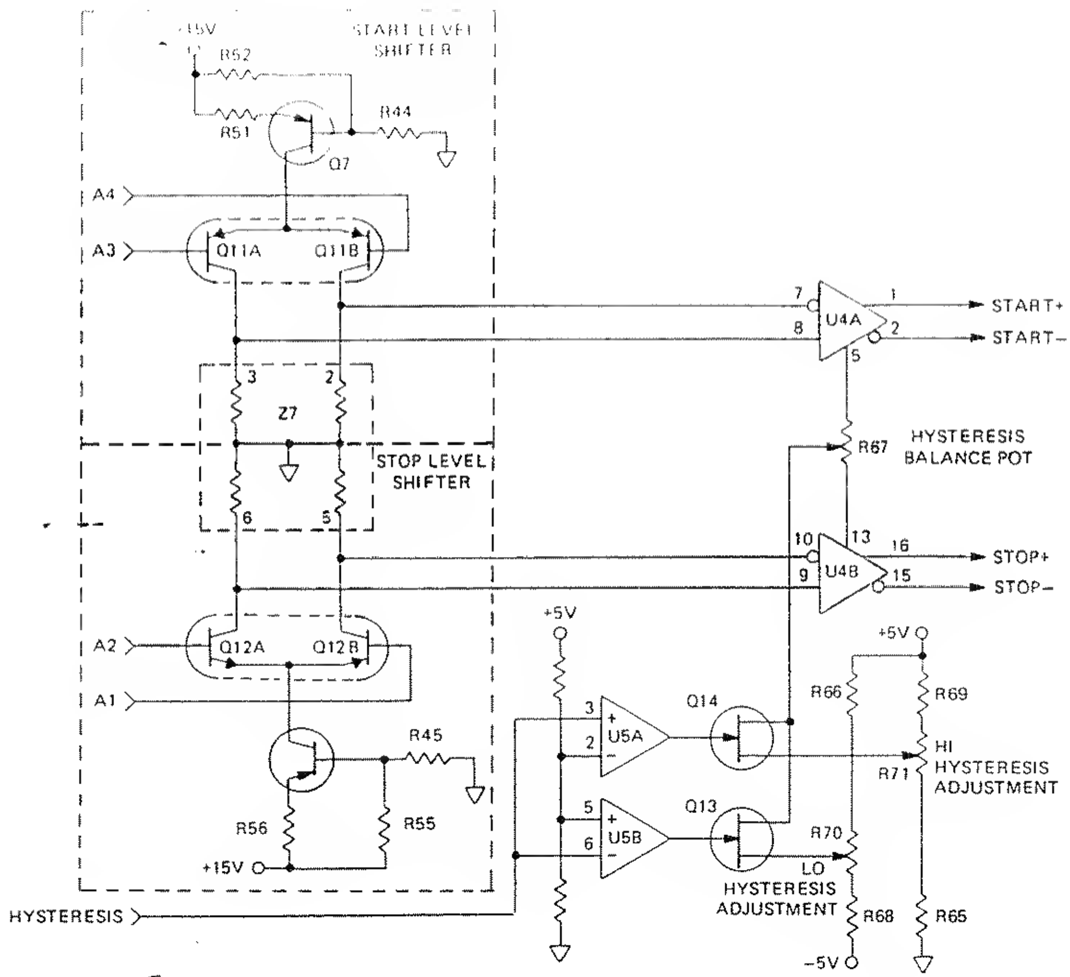


Figure 5.5 - Level Shifting and Hysteresis Control

5.3.2.2.6 Digital-to-Analog Converter (DAC) - Functional Description

5.3.2.2.6.1 Refer to Figure 5.6. The DAC block contains two identical circuits, the START DAC and the STOP DAC (START DAC only shown in figure). The DACs convert 12 bits of data from the microprocessor's 16-bit data bus into analog voltage used to program the start/stop buffer's trigger levels. These trigger levels are also routed to the rear panel for calibration purposes.

5.3.2.2.6.2 Each DAC consists of two sections: (1) a voltage section which performs the actual digital-to-analog conversion, and (2) a summing amplifier section.

5.3.2.2.7 START DAC Circuit Description

5.3.2.2.7.1 Refer to Figure 5.6. The following description refers only to the START DAC, but can also be applied to the STOP DAC.

5.3.2.2.7.2 The first half of the START DAC circuit, the voltage section, contains the DAC chip U19 and the operational amplifier feedback loop. U19 outputs a current dependent upon the 12-bit code which is input from the microprocessor. This current is converted into a negative voltage by the operational amplifier U23. This voltage is then applied to R19. R19, R20, U11A, and U20 all work together to convert this negative output into either a positive or negative DC level.

5.3.2.2.7.3 U19, a CMOS IC, receives a 12-bit word code from the microprocessor. The data bus, from where this word code is taken, is shared with many other devices, the DAC must be strobed by the microprocessor's chip select line $\overline{\text{STDAC}}$ and write line $\overline{\text{PWE}}$. When these two lines both go low, they latch the valid data code into U19.

5.3.2.2.7.4 U19 receives a reference voltage from U20. This voltage sets up the current through an internal resistor ladder-network either to ground at pin 2 or to the output at pin 1. The output current is dependent upon the binary code input to the 12 switches. With all data lines latched high, the current at pin 1 is equal to the input current at pin 19 (VREF). There are 4096 incremental steps of the signal level that can appear at the output proportional to the binary weighted input code.

5.3.2.2.7.5 U23 operates in a feedback configuration to act as a current-to-voltage converter. This feedback loop keeps the output voltage of the DAC (pin 1) at zero volts.

5.3.2.2.7.6 The voltage level at the output of U23 is always negative as a result of the signal inversion by operational amplifier U23. R19 and R20 constitute a voltage-divide network with U20 supplying +5 volts to R20 and R19 receiving its supply from the output of U23. As the voltage varies at R19, the amount of current will vary at point A (see Figure 5.6). The amount of current at U11's operational amplifier input will be amplified to achieve the START DAC voltage selected by the microprocessor's binary code. The gain of the summing circuit is about 3.16 and is established by R13, R14, R19 and R20.

5.3.2.2.7.7 The reference voltage input to the DAC is +5 volts and is supplied by U20. The output of the current-to-voltage converter of U23 ranges from zero to -5 volts. Since the DAC has 12 bits, it has the potential for 4096 current increments and its voltage resolution is about 1.2 millivolts. Because of the scaling of current and the gain setup of U11A, the DAC resolution is 2.5 millivolts per step. This provides a trigger level with a voltage range of +5.2 to -5.2 volts.

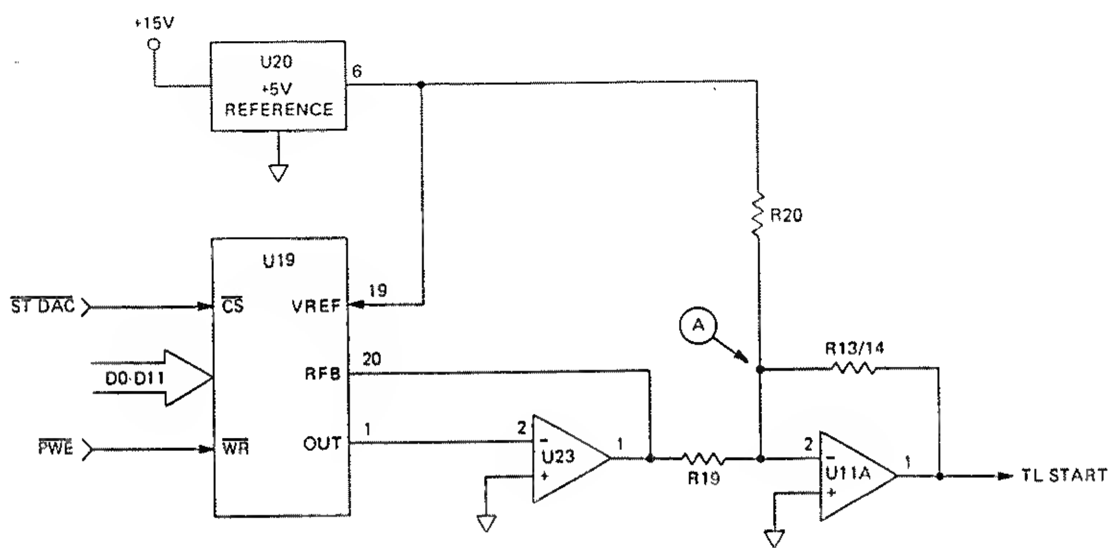


Figure 5.6 - Simplified Schematic for the START DAC

5.3.2.3 Auto-Trigger Circuitry

5.3.2.3.1 Functional Description

5.3.2.3.1.1 The auto-trigger circuit, in conjunction with the microprocessor and DAC circuitry, determines the amplitude of the input measurement signal for channel A and/or B. This is achieved by doing a signal peak search and then automatically setting the trigger level to the optimum 50% point. Depending on the trigger display selected (peak-to-peak, peak maximum, peak minimum, or the 50% point), this trigger value is then sent to channel A and/or B trigger displays on the front panel.

5.3.2.3.1.2 The peak signal search during auto-trigger determination actually involves a search for the positive and the negative peak levels. During each peak signal search, the microprocessor requires information regarding whether (1) the input signal crossed the trigger point that was set and whether (2) the input signal is above or below the trigger point. Now to a brief circuit description.

5.3.2.3.2 Circuit Description

5.3.2.3.2.1 Refer to Figure 5.7. To determine the trigger level automatically, information for calculation by the microprocessor is obtained from U30. When signal line $\overline{\text{CSBUFA}}$ is brought low, tri-state buffer U30 routes the Start Signal Crossing Level ($\overline{\text{STSXL}}$) and Start Signal Voltage Level (STSVL) signals to the microprocessor for reading.

5.3.2.3.2.2 The $\overline{\text{STSXL}}$ signal indicates whether the input measurement signal has crossed the trigger level. The $\overline{\text{STSLV}}$ signal indicates whether the trigger level is above or below the measurement signal. The microprocessor always looks at the $\overline{\text{STSXL}}$ signal first. If the $\overline{\text{STSXL}}$ signal level is high, the microprocessor looks at the $\overline{\text{STSLV}}$ signal to determine if the trigger level is set above or below the measurement signal. The microprocessor never looks at the $\overline{\text{STSLV}}$ signal if the $\overline{\text{STSXL}}$ signal is low because the microprocessor now has all the information to set the next trigger point.

5.3.2.3.2.3 Before the microprocessor can perform an auto-trigger, it first sets the DAC's trigger level to the start/stop amplifiers. Next, the auto-trigger circuitry is set up. First, the microprocessor brings the $\overline{\text{DLYWND}}$ and ARM signal lines high. This forces the ATE (Auto-Trigger Enable) line high and the $\overline{\text{ATE}}$ line low. This enables U54B and U55B.

5.3.2.3.2.4 With the DAC's trigger level and auto-trigger circuitry now set, the microprocessor initializes an auto-trigger process. The $\overline{\text{ATRST}}$ (Auto-Trigger Reset) signal line is first pulsed low, setting U55B's Q output high. If the DAC level was set within the measurement signal's peak-to-peak range, U55B's Q output would be clocked low by the ATSTART+ signal which is the buffered Start measurement signal. Once U55B's Q output has been brought low, U55B's Q output is fed back to the input at U58B-4. This maintains the D input to U55B at a low level which keeps U55B's Q output low during any more clock pulses from the ATSTART+ signal.

5.3.2.3.2.5 U54B and U55B's Q outputs $\overline{\text{STSXL}}$ and $\overline{\text{STSLV}}$ now pass to U53. U53 translates ECL signals to TTL signals, then passes the $\overline{\text{STSXL}}$ and $\overline{\text{STSLV}}$ signals to U30 for reading by the microprocessor.

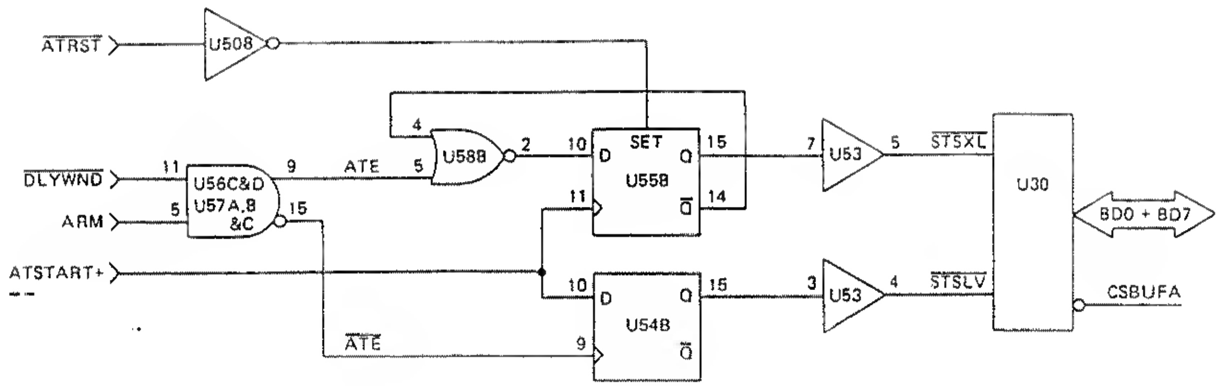


Figure 5.7 - Simplified Schematic for the Auto-Trigger Start Circuitry

5.3.3 Channel C Block

5.3.3.1 Functional Description

5.3.3.1.1 Channel C is provided on Model 1996 only. Refer to Figure 5.8 which provides a simplified block diagram. Channel C processes the signal applied at the channel C input and feeds it to the measurement block.

5.3.3.1.2 Channel C's input is protected by a fuse, mounted in the input connector, and also by a signal-limiting circuit. Next is an automatic level control circuit which reduces the range of the signal level applied to the amplifier.

5.3.3.1.3 After amplification, the signal is prescaled by 64 before being passed via a buffer and a signal gate to the measurement block.

5.3.3.1.4 The amplitude of the signal at the amplifier output is monitored by a detector and a comparator. The comparator output controls the low-signal latch. If the detector output is below the threshold, the latch is set and the channel output is inhibited by the signal gate. When the detector output goes above the threshold, the low-signal latch is armed and opens the signal gate on the next signal edge from the prescaler. This enables the instrument to make measurements on signal bursts.

5.3.3.1.5 The detector output is also applied to the continuous signal latch. This latch is reset at the beginning of each gate period and is set if the detector output falls below the threshold level. The microprocessor system samples the latch output throughout the gate period. If the measured signal falls below the threshold level during this period, the measured result is set to zero.

5.3.3.1.6 If channel C is not selected, the low-signal latch is held in reset by a control signal from the microprocessor and the output to the measurement block is inhibited. The same control signal is used to enable channel A so that the two channels cannot be enabled at the same time.

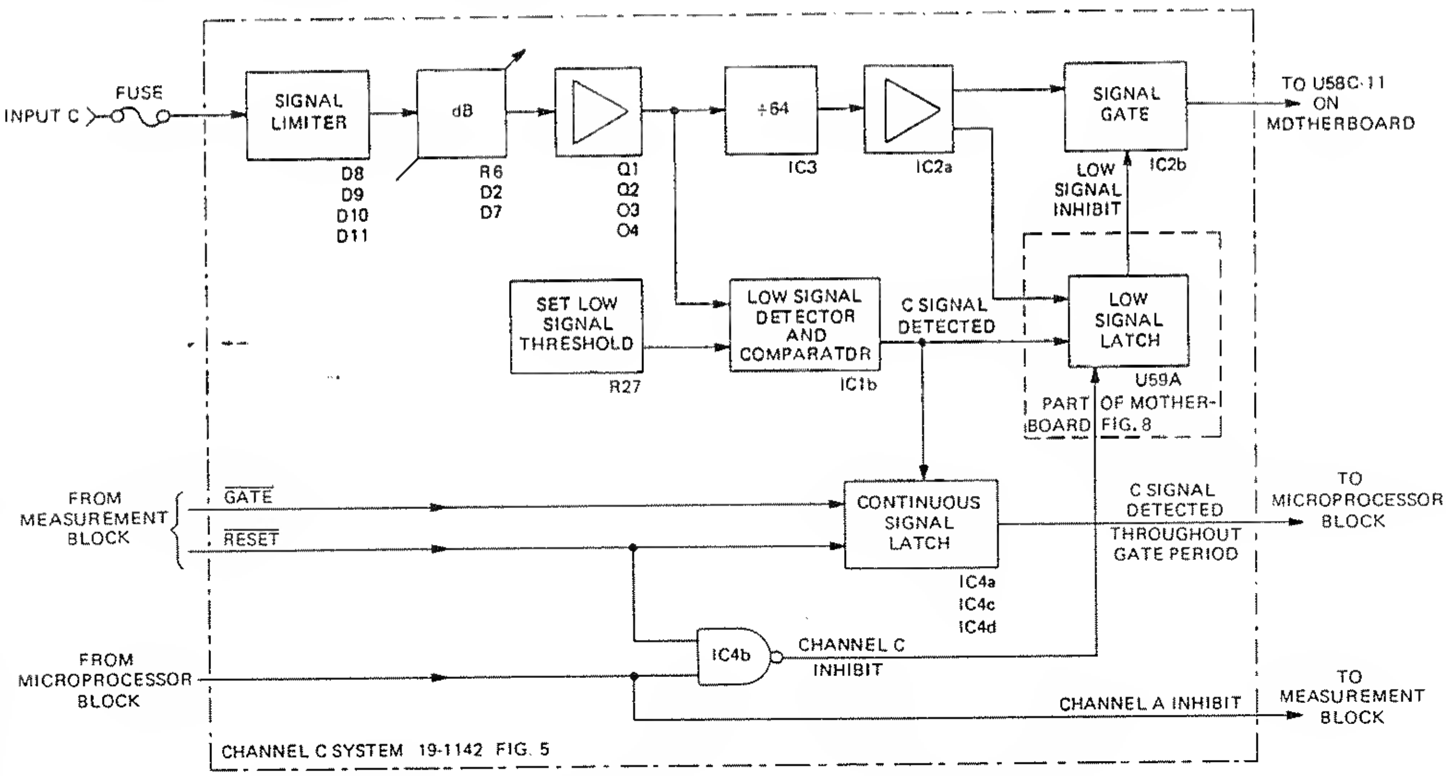


Figure 5.8 - Simplified Block Diagram for Channel C (1996)

5.3.3.2 Circuit Description

5.3.3.2.1 Refer to Section 7 for the complete channel C schematics. The signal to be measured is applied via SK13 (INPUT C). The circuit is protected by a fuse mounted within SK13. The signal amplitude is limited by the diode clamp comprised of D8, D9, D10 and D11.

5.3.3.2.2 A degree of automatic gain control is achieved by means of an attenuator formed by R6 and the impedance of the PIN diodes D2 and D7. The peak-to-peak detector D1, D3, R7 and C48 produces a negative voltage proportional to the signal amplitude. A direct current proportional to this voltage flows through the PIN diodes via L1. The impedance of the diodes decreases if the current increases so that changes in signal amplitude are offset by changes in attenuation.

5.3.3.2.3 The signal passes through four amplifier stages incorporating Q1, Q2, Q3 and Q4. The amplified signal is fed to the counter IC3 via the shaping circuit formed by R37, C46 and R36.

5.3.3.2.4 The signal frequency is prescaled by 64 in IC3 and buffered in IC2a. Provided that channel C is selected and the amplitude of the signal is adequate, the output at IC2a-2 passes to the measurement logic via the gate IC2b and SK7 pin 5.

5.3.3.2.5 The signal at the output of Q4 is fed to the low-signal detector D5 and C23. The comparator IC1b compares the detector output with a threshold voltage set by R27. The comparator output is at a logic 1 if the detector output is below the threshold (the amplitude of channel C's signal is too low for accurate counting).

5.3.3.2.6 The logic level at the comparator output is inverted in IC1-A and is fed via SK7 pin 14 to the D1 input of U59A-7 on the motherboard. U59A-6 is clocked by the output of IC2a via SK7 pin 8. If the signal from Q4 is below the threshold, U59A-3 goes to a logic 1. This logic level is fed back via SK7 pin 7 to disable the gate IC2-B and inhibit the output to the measurement block.

5.3.3.2.7 The $\overline{\text{GATE}}$ signal enters the system at SK7 pin 17 and is inverted in IC1-C. The resulting signal and the output of the comparator IC1-B are fed to IC4-A. If both inputs are at a logic 1, indicating that the channel C level is too low while the gate is open, the continuous signal latch IC4-C and IC4-D is set. The latch output is fed to the microprocessor via SK7 pin 11 and prevents the result of any measurement made during that gate period from being displayed.

5.3.3.2.8 The STSL signal at SK7 pin 16 is at a logic 1 when channel C is selected. When channel C is not selected, SK7 pin 16 is at a logic 0. This level is inverted and buffered in IC4-B and IC1-D, and then is fed to U59A-4 (see channel C schematic) via SK7 pin 13. U59A-4 is held reset, inhibiting the channel C signal at IC2-B via SK7 pin 7.

5.3.4 Measurement Logic Block

5.3.4.1 Functional Description

5.3.4.1.1 Refer to Figure 5.1 and 5.9 when reading this description of the measurement logic block.

5.3.4.1.2 The start and stop signals after signal conditioning are applied first to the divider/multiplexer and auto-trigger circuitry (see figure). The multiplexer selects either the start divide-by-2 or the start/stop signals.

5.3.4.1.3 The synchronization circuit is designed to delay the start and stop signals' clocking edge from reaching the MCC2 chip (U6) before the start enable (STEN) and stop enable (SPEN) control signals. After synchronization, the start and stop signals are applied to ECL LSI device U6 along with the reference signal and start and stop enable control signals.

5.3.4.1.3.1 The start enable and stop enable signals define the gate time. The start enable control signal is generated by the CPU or external Input A, B or D; the stop enable control signal follows the start enable signal by a time determined by the gate circuitry.

5.3.4.1.3.2 The reference signal is provided by either a precision 10 MHz oscillator or an external reference signal of 1, 5, or 10 MHz at 500 mVrms to 5 Vrms.

5.3.4.1.4 The ECL LSI device executes a partial reading conversion and passes the information to CMOS LSI device U11. Additional information from the ECL LSI device is directed to the precision TEC assembly U10 which performs a precision timing-error-correction operation. The TEC assembly then passes the information from timing error correction to the CMOS LSI device.

5.3.4.1.4.1 This latter device (U11) performs the remaining reading conversion and also presents the results on the data lines when interrogated by the CPU. The CPU then executes the appropriate function-dependent calculations, displaying the measurement results on the instrument's front-panel display.

5.3.4.2 Divider/Multiplexer Circuit Description

5.3.4.2.1 Refer to Figures 5.5 and 5.9 for the following circuit description.

5.3.4.2.2 The four differential output signals from U4 are directed to U7 and U6. One of these, the START+ signal from U4A-1, also passes to the clock input of U8A. U8A (a D-type flip-flop) functions by dividing this clock-input START+ signal by two.

5.3.4.2.3 Q and $\overline{Q}$ are the two outputs of U8A comprising the complementary outputs of the divided START+ signal. Q and $\overline{Q}$ are then routed to U7, a two quad-channel multiplexer.

5.3.4.2.4 U7 selects either the complementary input of the start and stop signals from U4A and B, or the Q and $\overline{Q}$ signals from U8A for presence at its outputs. Selection is effected via the $\overline{\text{200 MHz}}$ ECL control line.

5.3.4.2.5 The $\overline{\text{200 MHz}}$ control signal goes to U8A and U7. U8A will only divide the START+ signal at its clock input when both the $\overline{\text{200 MHz}}$ and Q1 signals at U8A are at an ECL low. This condition permits the START+ signal at U8A's clock input to be divided and routed through U7 to its complementary outputs.

5.3.4.2.6 However, when the $\overline{\text{200 MHz}}$ signal at U7 and U8A is at an ECL high, the divide path is disabled. Then the complementary outputs from U4A and B are selected to pass through U7 to its complementary outputs.

5.3.4.3 Synchronization Circuit Description

5.3.4.3.1 Refer to Figures 5.5 and 5.9, and especially 5.10 for the following circuit description. This description is confined to the START+ SYNC circuit as the STOP+ SYNC circuit is essentially the same.

5.3.4.3.2 The START+ input signal is connected to U4A, which is an exclusive-or gate with complementary output. U4A selects the slope of the START+ signal at U4A-7 by setting U4A-9 at an ECL logic level.

5.3.4.3.3 Slope selection is effected by the TTL control signal STSL. When this control line goes low at U3A, the latter converts the TTL signal to an ECL low. U3A's ECL level drives U4A-9 to a corresponding low ECL level. This selects the positive slope of the START+ signal to be at U4A's output.

5.3.4.3.4 When control line STSL is high, the negative slope of the START+ signal is selected to be at U4A's output.

5.3.4.3.5 The complementary outputs of U4A are connected to the latch enable lines of U7A. These latch enable lines (U7A-5 and 6) enable or disable the STEN signal to pass through U7A to Q2 and Q4. See Figure 5.10.

5.3.4.3.6 Q2 and Q4 take the complementary ECL outputs from U7A and convert the ECL level to a TTL level at the collector side of Q2. This signal is named DSTEN.

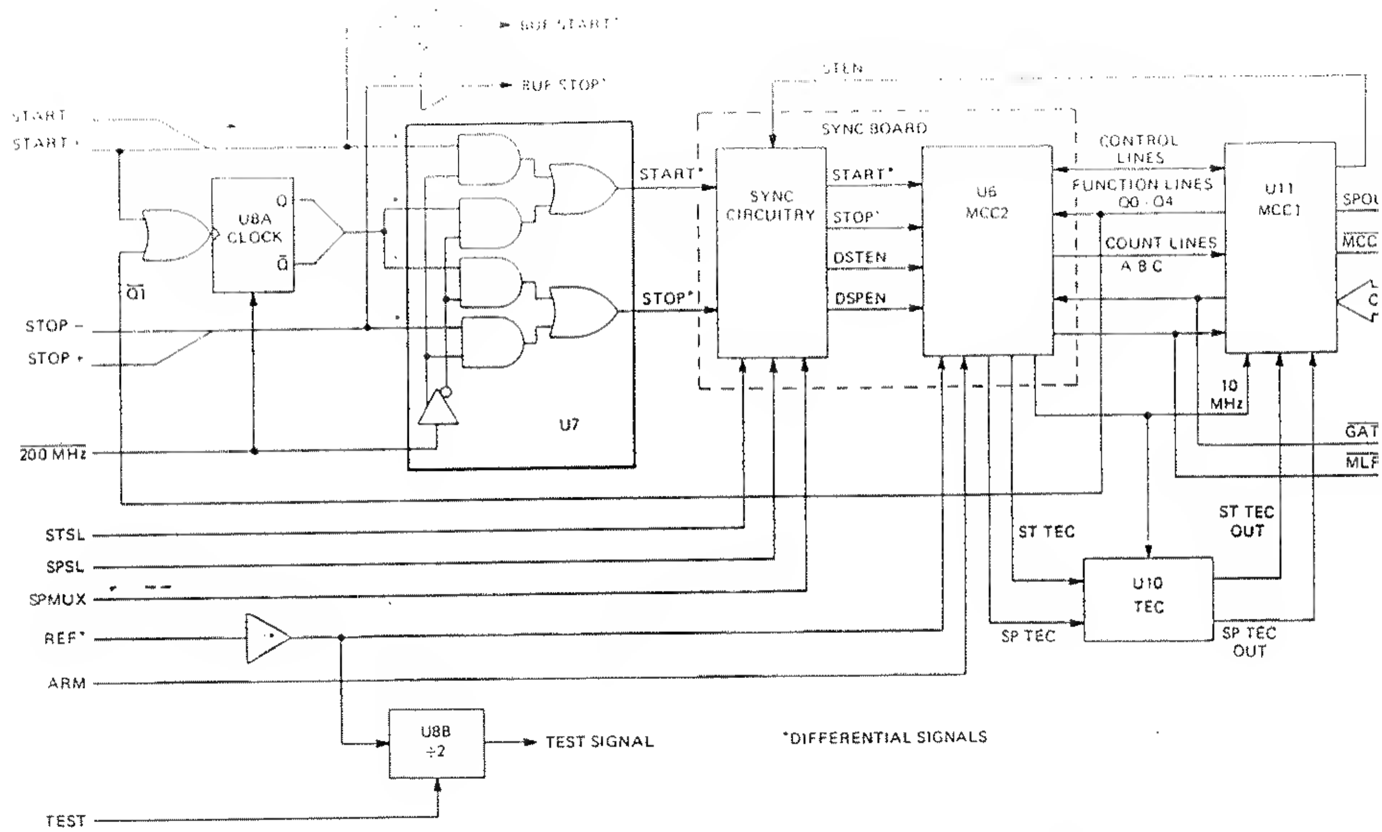


Figure 5.9 - Simplified Diagram for the Measurement Logic Block

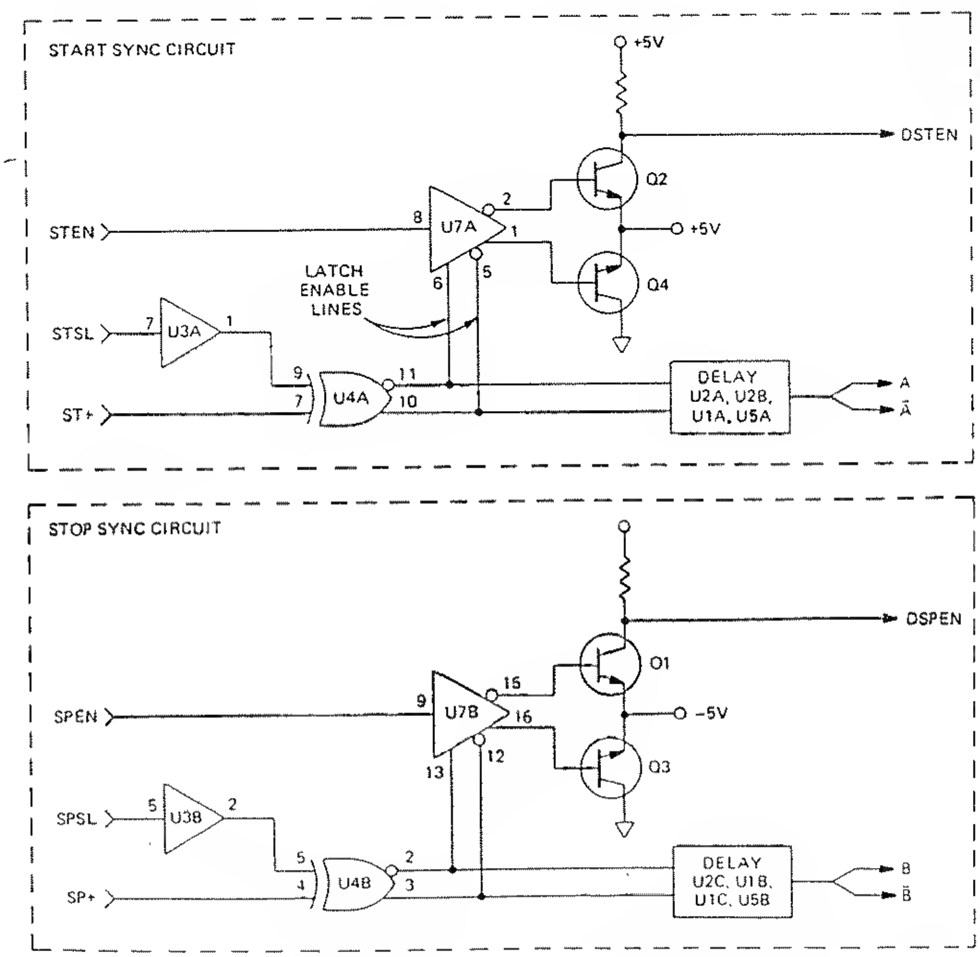


Figure 5.10 - Simplified Schematic for the Synchronization Circuit

5.3.4.4 Measurement Circuit Description

5.3.4.4.1 Refer to Figure 5.9 for the following description of the measurement circuit.

5.3.4.4.2 The measurement circuit consists essentially of the three chips, U6, U10, and U11. U6 is the chip where the input signals from channels A, B and C enter for measurement after signal conditioning. U11 is a CMOS chip and the heart of the measurement circuit. This IC receives all control functions for signal measurement from the microprocessor and, also under microprocessor control, enables a reading to be taken.

5.3.4.4.3 A reading takes place when the microprocessor sets up the function control lines Q0 through Q4 of U11. These control lines are connected from U11 to U6 to direct the input signal(s) through U6's internal logic.

5.3.4.4.4 When the microprocessor is ready, it orders U11 to set the STEN line high. However, this control line cannot go high yet as it has to wait to be clocked high by the 10 MHz timing signal from U6. When the STEN line does go high, it is routed to the synchronization circuit where it is converted to the DSTEN signal. It is the DSTEN signal which goes to U6, enabling a measurement to begin on the first clocking edge of the input signal to U6.

5.3.4.4.5 When U6's internal logic sees the clocking edge of the input signal(s), the ST TEC line from U6 to U10 goes low and so does the $\overline{\text{GATE}}$ line to U6. From 100 to 200 nanoseconds later the REF signal will clock the ST TEC line high.

5.3.4.4.6 Once the measurement begins, count lines A, B and C from U6 to U11 start to toggle. These three lines carry the least significant bits of a counter register that is 26 bits in length. The 23 most significant bits are stored in U11. At the end of the measurement, the DSPEN line at U6 goes high. This enables U6's internal logic to stop the measurement on the next clocking edge of the input signal at U6.

5.3.4.4.7 When U6's internal logic sees the input signal(s) next clocking edge, the SP TEC line from U6 to U10 will go low and the $\overline{\text{GATE}}$ line high. From 100 to 200 nanoseconds later, the REF signal will clock the SP TEC line high.

5.3.4.4.8 The ST TEC and SP TEC signals from U6 to U10 are both ECL low-going pulses. Each lasts from 100 to 200 nanoseconds. This pulse width represents the time difference (an error factor) between the clocking edge of the input signal and the 10 MHz reference signal. Refer to Figure 5.11.

5.3.4.4.9 U10 uses the ST TEC and SP TEC pulses in a dual-slope integration scheme. Using a constant current source, both pulses rapidly charge a capacitor. When the pulses end, the capacitor starts a scaled discharge at about 1/400th of the charge rate. This proportionally expands the TEC error pulse by a factor of 400. This integrated waveshape is then squared and used to gate the 10 MHz reference signal (the ST TEC OUT and SP TEC OUT signals) into U11's TEC register counters. Refer again to Figure 5.11.

5.3.4.4.10 At the end of a measurement,the CPU commands U11 to set the MLRST line low. This line resets all logic and register counters in U6 and U11, preparing for the next measurement.

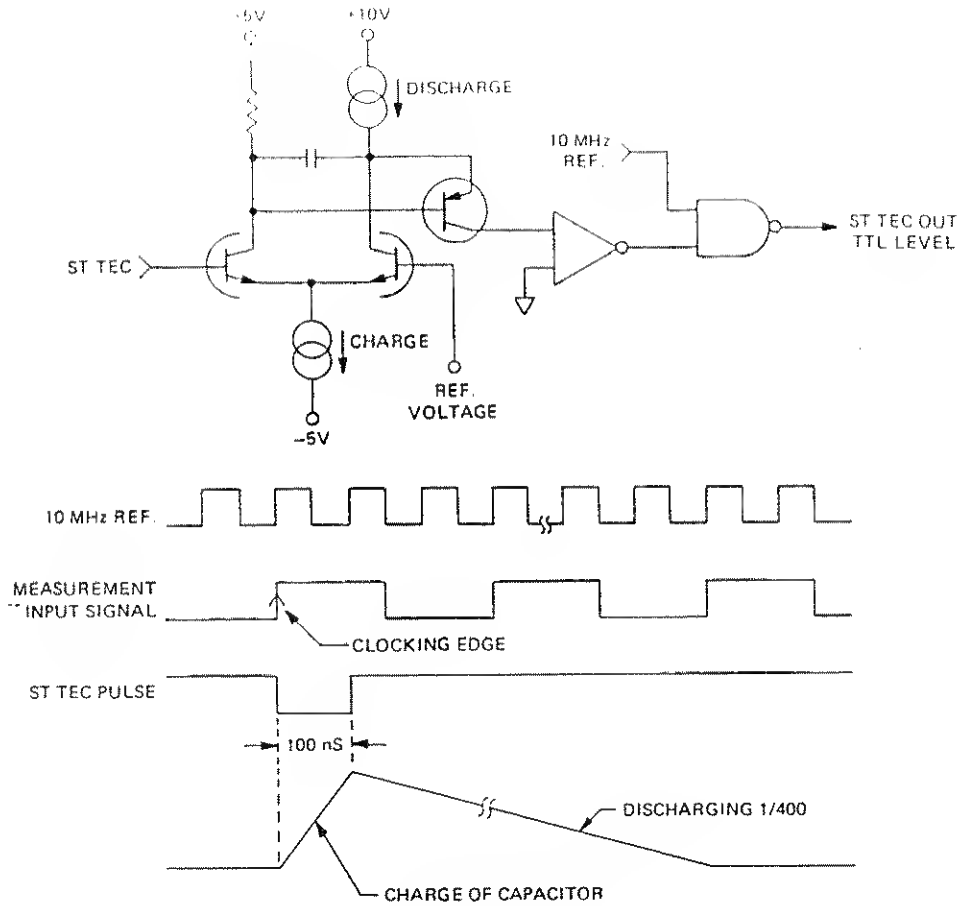


Figure 5.11 - Simplified Diagram of the TEC Interpolator

5.3.5 Display/Keyboard Block

5.3.5.1 Functional Description

5.3.5.1.1 Refer to Figure 5.12. The front panel contains the display and keyboard circuitry. It has all the operator pushbutton controls for all counter functions, and displays measurement readings and diagnostic data such as errors and failure codes.

5.3.5.1.2 The front panel provides eleven 7-segment LEDs, 53 red LEDs, and two 4-digit trigger-level displays for channels A and B. Ten of the 7-segment LEDs are used for the mantissa. The eleventh 7-segment LED is the measurement reading exponent.

5.3.5.1.3 The keyboard has 40 momentary-contact pushbutton switches. It is continuously monitored via a 7 x 6 line matrix. ROW1 through ROW6 are strobed by a 3-to-8 line decoder/multiplexer. COL1 through COL7 are scanned and read from the data bus via a buffer.

5.3.5.2 Circuit Description

5.3.5.2.1 Refer to Figure 5.12. The display board receives its instructions from the microprocessor through chips U3, U5, U6, U7 and U8. U3, U5 and U6 control display drivers U1, U2 and U4 as well as ten miscellaneous function/indicator LEDs. The microprocessor interfaces with the keyboard via chips U7 and U8.

5.3.5.2.2 Display drivers U1, U2 and U4 are Intersil (ICM7218) 8-digit LED devices. This device contains an 8 x 8 static memory array providing storage for the displayed information of the 7-segment decoders, all the multiplex scan circuitry, and high-power digit and segment drivers. The display driver has two control lines ($\overline{\text{WRITE}}$ and MODE) that define the chip select. The chip select either reads four bits of control information (DE, DF, DG or DH) or eight bits of display input data (DA through DH). The MODE control line defines the selection, with a high loading the control word on the write pulse, or a low loading the input data on the write pulse.

5.3.5.2.3 Any data present (BD0 through BD7) at the input of U3, U5 and U6 is latched out on the rising clock edge of lines CSLCHF, CSLCHG and CSLCHH. U5 handles the control lines (MODE, $\overline{\text{WRU1}}$, $\overline{\text{WRU2}}$ and $\overline{\text{WRU4}}$) and U3 handles the data lines (DA through DH) for the display drivers. Drivers U1 and U2 show the mantissa readings on the 7-segment display DS1 through DS11, and driver U4 shows channel A/B trigger levels on display DS12 and DS13.

5.3.5.2.4 The microprocessor refreshes the counter's measurement readings (mantissa) about every millisecond. Every time the display is updated by the microprocessor, the microprocessor must pass the mode data along with eight consecutive bytes of data for each of the three display drivers.

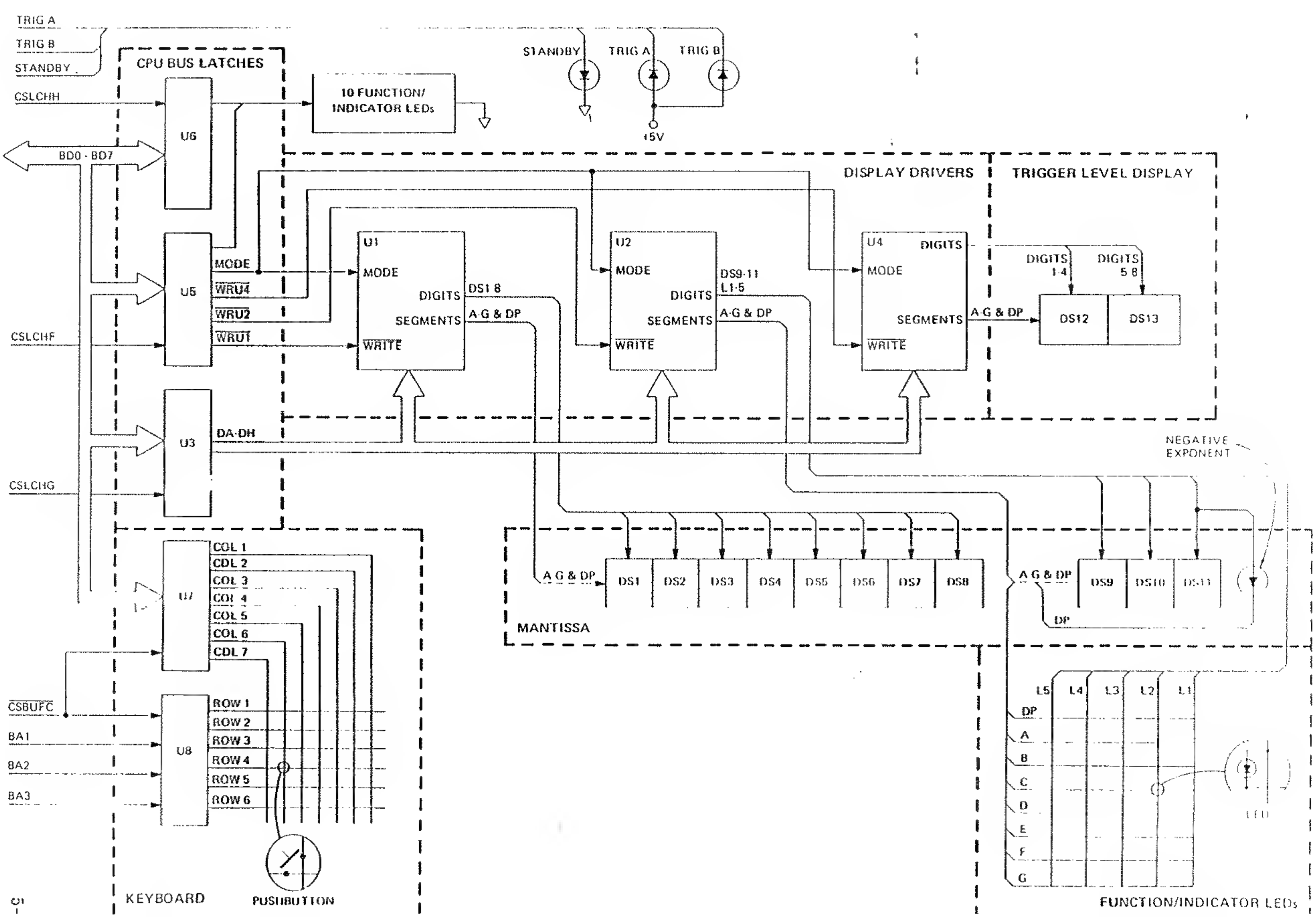
5.3.5.2.5 Mode data is passed to U1, U2 or U4 when the MODE control line from U5 is high and the $\overline{\text{Write}}$ line ($\overline{\text{WRU1}}$, $\overline{\text{WRU2}}$ or $\overline{\text{WRU4}}$) goes low. Lines DE, DF, DG and DH contain the control word that will be loaded into the display drivers.

5.3.5.2.6 Display data is passed when the MODE control line is low and the appropriate $\overline{\text{Write}}$ line goes low. Lines DA through DH now carry the display data for the mantissa and function/indicator LEDs. All display data directed to U1, U2 and U4 is coded in hexadecimal.

5.3.5.2.7 The function/indicator LEDs are controlled by U6, a part of U5, and the last five digit lines of U2 (L1 through L5).

5.3.5.2.8 The keyboard is scanned about every ten milliseconds. Scanning is effected by sequencing through BA1, BA2 and BA3; bring line $\overline{\text{CSBUFC}}$ low; and then reading buffer chip U7. It takes the microprocessor eight passes to read all 40 keys. For example, in order for the microprocessor to read ROW4 and COL6, lines BA1 and BA3 will be set high and line BA2 will be set low. The microprocessor next would bring line $\overline{\text{CSBUFC}}$ low, enabling U8 to bring the ROW4 line low. If the key across ROW4 and COL6 is depressed, COL6 will be low and the microprocessor will read via buffer chip U7 the value BF in hexadecimal. If that key is not depressed, the microprocessor will read an FF instead.

Figure 5.12 – Simplified Schematic for the Display Board



5.3.6 Microprocessor Block

5.3.6.1 Functional Description

5.3.6.1.1 Refer to Figure 5.1. The overall operation of the 1995/1996 is controlled by the microprocessor which resides in the computer section on the motherboard. The microprocessor itself is a Motorola 68000 device. It receives instructions from the keyboard or the GPIB, then sends instructions to and receives data from other functional blocks within the counter.

5.3.6.1.2 The microprocessor continuously scans the counter's keyboard for any change and then updates the front-panel display annunciators and key indicators.

5.3.6.1.3 The microprocessor block contains eight major divisions. Refer to Figure 5.13. These divisions include the following:

a. Upper and lower RAM (U7 and U8)

b. Upper and lower ROM (U17 and U18)

c. Non-volatile memory

d. Microprocessor control logic

e. Reset logic

f. Interrupt logic

g. Address and data buffer

h. Input/Output decoders

5.3.6.1.4 The microprocessor interfaces to these eight divisions via a 16-bit data bus and a 24-bit address bus. All input/output functions are effected via an 8-bit data bus and a 4-bit address bus. The address bus interfaces with the measurement block, GPIB block, display block, and hardware control circuitry.

5.3.6.1.5 The microprocessor has 16k bytes of RAM and 128k bytes of ROM available for memory.

5.3.6.2 **Circuit Description**

5.3.6.2.1 Microprocessor Control Circuitry

5.3.6.2.1.1 The clock (hybrid IC) U16 provides an 8 MHz clock to the microprocessor U6. The control circuitry of U6 consists of inverter U5, NAND gate U4, and OR gates U24 and U25. These devices develop all the control signals listed in Table 5.1 for the microprocessor, permitting it to interface with peripheral devices within and without the kernel.

5.3.6.2.2 Reset Circuitry

5.3.6.2.2.1 The reset circuitry consists of the power-down and power-up circuits. The power-down circuit brings the output of U1C (RESET) low when U1C-11 reaches approximately 4.7 volts. This prevents the microprocessor from accidentally writing to non-volatile memory. The power-up circuit holds the output of U1B ($\overline{\text{RESET}}$) low until U1C-11's voltage is greater than 1.2 volts. Q1 is the turnoff which permits C2 to begin charging. When C2 reaches a charge that is greater than 1.2 volts, the output of U1B will go high, enabling the microprocessor and other peripherals to return from their reset state.

5.3.6.2.3 ROM

5.3.6.2.3.1 U17 and U18 are EPROMs containing the resident operating-system. This information is accessed by the microprocessor through a 16-bit data bus and a 24-bit address bus. However, only 14 of the 24 address lines are used (A1 through A15). The microprocessor divides the data bus into upper and lower data lines. U17 is connected to the upper 8 bits (D8 through D15), while U18 is connected to the lower 8 bits (D0 through D7). To enable a data output (read) cycle, both $\overline{\text{UDE}}$, $\overline{\text{LDE}}$ and address line A17 are pulled low. Instruction bytes are then put onto the data bus.

5.3.6.2.4 RAM

5.3.6.2.4.1 U7 and U8 are static RAM devices that provide 8k x 16 bits of temporary storage. This information is also accessed by the microprocessor through a 16-bit data bus and a 24-bit address bus. However, only 12 of the 24 address lines are used (A1 through A13). U7 is connected to the upper 8 bits (D8 through D15), while U8 is connected to the lower 8 bits (D0 through D7). To enable a data input (write) cycle, the $\overline{\text{RAMENA}}$, $\overline{\text{LWE}}$ and $\overline{\text{UDE}}$ lines are pulled low. To enable a data output (read) cycle, the $\overline{\text{LWE}}$ line remains high, while the $\overline{\text{RAMENA}}$ and $\overline{\text{UDE}}$ lines are pulled low.

5.3.6.2.5 Non-Volatile Memory

5.3.6.2.5.1 U2 provides 2k x 8 bytes of non-volatile memory storage for calibration constants and machine setups. U2 is connected to the lower half of the data bus (D0 through D7) and A1 through A11 of the address bus. To enable a data input (write) cycle, chip select line $\overline{\text{CSNONVOL}}$, $\overline{\text{LDE}}$ and the output of U3A are pulled low. To enable a data output (read) cycle, the output of U3A remains high while the $\overline{\text{CSNONVOL}}$ and $\overline{\text{LDE}}$ lines are pulled low. This read/write cycle of non-vol memory involves only the lower 1k of U2's memory. The write cycle of the microprocessor is unable to access the upper 1k of U2's memory because U3A, U3B and the calibration switch on the front panel inhibit this write cycle. This ensures protection to the calibration constants which are stored in the upper half of U2's address space.

5.3.6.2.6 Input/Output Decoder Circuit

5.3.6.2.6.1 The input/output decoders consist of the three 3-to-8 multiplexers U9, U15 and U22. These three chips provide the chip select lines and clock signal for the peripheral devices. Refer to Table 5.1 for a definition of the chip select clock names.

5.3.6.2.7 Interrupt Circuit

5.3.6.2.7.1 This circuit consists of one chip, U12, which is an 8-to-3 line priority encoder. This IC handles the interrupt lines from the measurement block ($\overline{\text{MCCIRQ}}$), GPIB block, timer and gating block ($\overline{\text{RTIRQ}}$), and optional interrupts ($\overline{\text{OPTIRQ}}$). These interrupt lines are prioritized, then a 3-line code is sent to the microprocessor.

5.3.6.2.8 Address and Data Buffer

5.3.6.2.8.1 U26 is a bidirectional buffer that buffers data lines D0 through D7 from the microprocessor to the measurement block, display bloek, GPIB block, and hardware control circuitry. This buffer chip is only enabled when reading and writing from peripheral devices outside the kernel. U27 buffers address lines A1 through A4.

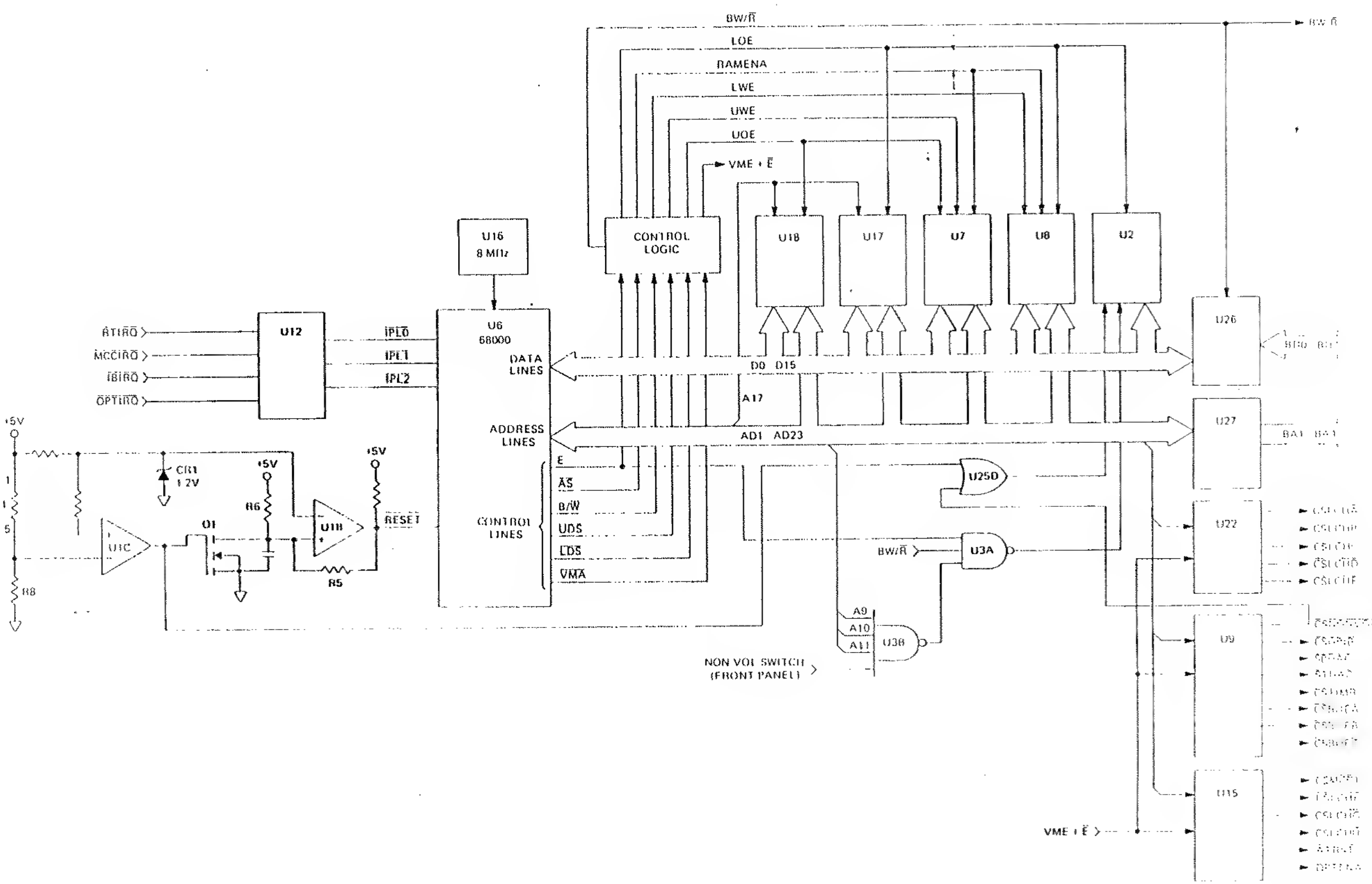


Figure 5.13 – Simplified Schematic for the Microprocessor Block

5.3.7 Power Supply Block

5.3.7.1 The 1995/1996 uses a linear power supply providing the following voltages (±5%) at the indicated current capacities:

a. +5V at 750 mA surge, 350 mA nominal (using ovenized oscillator Option 04E)

b. +5V at 3.2A (TTL)

c. -5.2V at 2.8A (ECL)

d. +15V at 250 mA (Linear)

e. -15V at 100 mA (Linear)

5.3.7.2 -- Line voltage enters the power transformer's primary winding when rear-panel connector S200 is closed. The line voltage selector card is oriented by the user to properly configure the primary winding to match the applied line voltage (see Subsection 2.7.2 in this manual for details).

5.3.7.3 The power transformer is a step-down device with three center-tapped secondary windings. Power transformer output voltages are full-wave, rectified by bridges CR8, CR200, and diodes CR10, CR11, before being capacitor filtered.

5.3.7.4 When switch S1 is closed, the positive and negative 15V supplies come up. The +15V supply enables the +5V TTL supply via Q7. The computer resets and, upon a successful completion of a status check, turns on the -5.2V supply via Q5, Q8 and Q9. When switch S1 is opened, all power supplies shut down except the oven oscillator supply. Q4 turns on and lights the front-panel Standby LED.

5.3.7.5 The +5V TTL and -5.2V ECL power supplies are overvoltage/current protected by thyristors Q10 and Q11. The FANRUN line remains at approximately .7V when the fan is operating. If no current flows through the fan, U1-2 goes low forcing BD5 low when U13 is addressed by the computer. The computer then turns off the -5.2V supply, thereby reducing internal heat dissipation to a safe level.

5.3.8 External Arming/Gating Block

5.3.8.1 Funtional Description

5.3.8.1.1 The 1995/1996 provides special circuitry permitting control of the measurement gate start and stop time by external means. Measurement gate control in normal operation is a function of the selected measurement mode and input channel(s). External arming and gating is provided by channels A, B, and rear-input D. Thus, a variety of arming and gating signals can be used.

5.3.8.1.2 When in one of the external arming/gating modes, the microprocessor illuminates the EXT LED on the front panel, indicating that the counter is set up for receiving an external arming/gating signal via channel A, B or D.

5.3.8.1.3 The external gating signal defines the beginning (Start) and end (Stop) of the measurement. In using the external gating signal, one of four slope combinations can be selected: positive-to-positive, positive-to-negative, negative-to-negative, and negative-to-positive.

5.3.8.1.4 The external arming signal defines the beginning (Start) of the measurement; the end (Stop) is defined by the internal gate-time setting. Positive and negative slope selections are possible in the external arming mode.

5.3.8.1.5 In addition, the synchronous window auto-trigger (SWAT) mode may be selected. SWAT, which uses the external arming/gating circuitry, permits the auto-trigger to function only within a specified window. For example, the window can be set between possible ringing on both the rising and falling edges of the input measurement signal. Measurements are then taken only during this window, resulting in much more accurate readings. The only difference between the external gating mode and SWAT is that the gate signal is sent to the auto-trigger circuitry between measurements when in the SWAT mode.

5.3.8.2 Circuit Description

5.3.8.2.1 Refer to Figure 5.14. The arming and gating controls are set up via two latches, U29 and U31. U29 controls several control signal lines for the arming and gating circuitry which are SELSP, SELCHD, ARMSYNC, and SELARM. SELSP and SELCHD control the selection of channel A, B or D as the external arming or gating signal. SELARM enables the arming or gating signal to pass on to the auto-trigger circuitry or the measurement circuitry. ARMSYNC synchronizes the external arming or gating signal with the measurement circuitry. U31, ARMSTSL, and ARMSPSL controls the arming or gating slopes of the selected signal (Channel A, B, or D).

5.3.8.2.2 U40A serves as a 2-to-1 line signal selector/multiplier. It selects either the TTLSTOP (channel A/B input) or CHANLD (channel D input) signal. The TTLSTOP signal is selected to appear at the output of U40A when control signal SELSP is high and SELCHD is low from U29. The CHANLD signal is selected when the SELSP is low and SELCHD is high. Selected signal TTLSTOP or CHANLD is then passed from the input of U40A to the input of U32A and U32B for slope selection.

5.3.8.2.3 U32A and B is an exclusive-or gate with U32A selecting the start slope and U32B selecting the stop slope of the arming or gating signal. A logic high on the ARMSTSL or ARMSPSL line selects the positive slope for clocking U43A and B. A logic low on ARMSTSL or ARMSPSL selects the negative slope. With a selected arming mode, only the ARMSTSL is used to initialize a measurement.

5.3.8.2.4 U43A and B is a D-type, positive-edge trigger flip-flop. U43A's flip-flop circuit controls the rising edge of the ARM signal and U43B's flip-flop circuit controls the falling edge. With an arming mode, only the rising edge of the ARM signal is processed by the measurement block to start a given measurement. With a gating mode, both the rising and the falling edge of the ARM signal is processed by the measurement block to both start and stop a measurement.

5.3.8.2.5 When the microprocessor brings the ARMSYNC signal high, U43A's Clear (CLR) line is released. With the CLR line high, the output of U32A (ARMSTART) clocks U43A's input, forcing U43A's Q output high and $\bar{Q}$ output low. This low is passed to U37A-10, with U37A-9 low; the output of U37A will go from a high to a low. This low from U37A-8 is passed to U39-1 if U42B-4's SELARM is enabled (high). U39A inverts the $\overline{ARM}$ signal to ARM and passes it to the measurement block. The rising edge of the ARM signal arms U6 to start a measurement.

5.3.8.2.6 U43B is held disabled by U43A's Q output until U43A's ARMSTART signal clocks Q high. Once U43B is enabled, U43A's Q output is passed to U43B's D input. When the clock edge of the ARMSTOP signal clocks U43B, U43B's Q output will go high and the $\bar{Q}$ output will go low. The Q output of U43B is then passed through U37A and U42B to the input of U39A. U39A inverts the high to a low and passes it to the measurement block causing the falling edge of the ARM signal to stop the measurement. U43B's Q output is fed back to U43A's Clear input resetting Q and $\bar{Q}$ and disabling U43B.

5.3.8.2.7 At the end of the measurement, the microprocessor brings the ARMSYNC line low. This disables the arm and gate circuitry until the microprocessor brings the ARMSYNC line high again to start a new measurement.

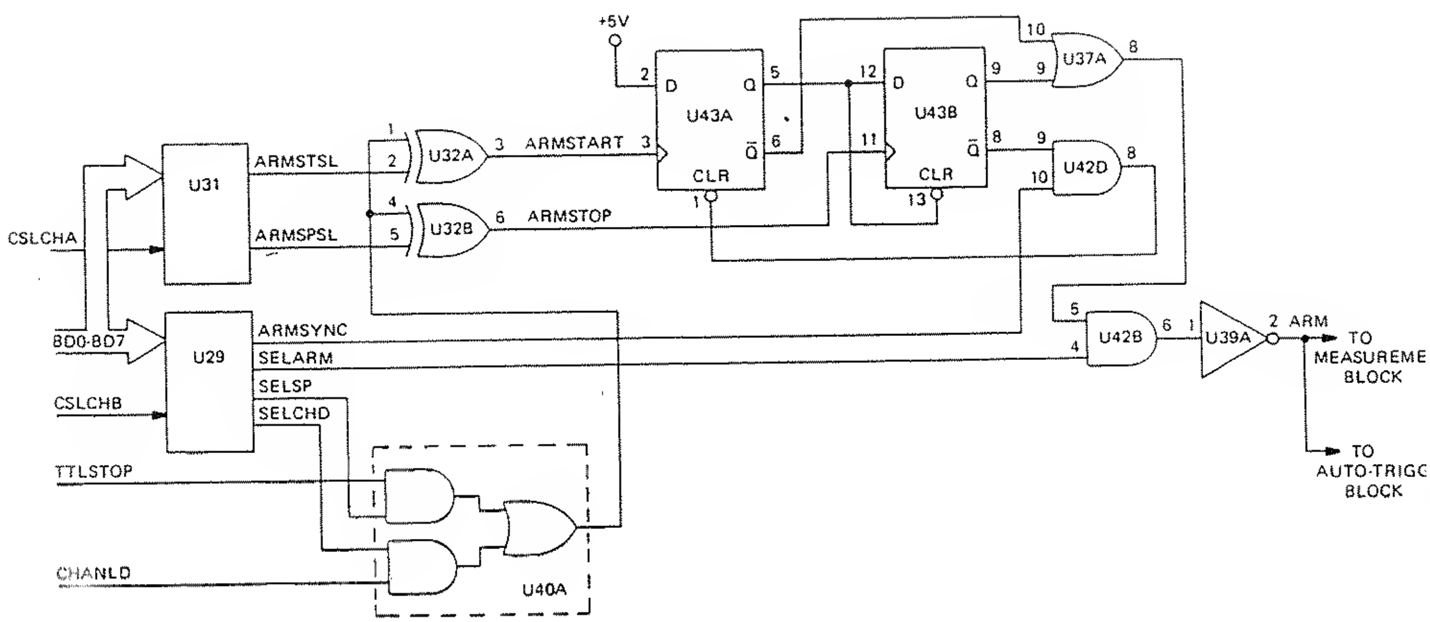


Figure 5.14 - Simplified Diagram for the External Arming/Gating Block

5.3.9 Internal Gate Timer Block

5.3.9.1 Functional Description

5.3.9.1.1 Refer to Figure 5.15. The gate timer controls two functions: (1) real-time interrupts and (2) gate time. U28 is a programmable interval timer that has three independent 16-bit counters. One is used for real-time interrupts, and the other two are cascaded together as the gate timer.

5.3.9.1.2 The timer for real-time interrupts is programmed to interrupt the microprocessor every ten milliseconds. Programming for this counter is effected at power-up and is not changed.

5.3.9.1.3 The gate time is changed whenever the function, resolution, or a new gate time is programmed by the user. 1995/1996 gate times can be programmed as short as 200 nanoseconds or one cycle of the measurement signal to 100 seconds.

5.3.9.1.4 The gate timer block controls the end of a measurement. Depending on the counter's chosen measurement function, the counter will select the gate-ending signal which is either created by the timer chip U28 or the MCC1 chip in the measurement block.

5.3.9.2 **Circuit Description**

5.3.9.2.1 Refer to Figure 5.15. The end of a measurement can be controlled by either the SPOUT or $\overline{\text{GATE END}}$ signals. SPOUT is generated by the MCC2 (U11) of the measurement block and is connected to U41-2. $\overline{\text{GATE END}}$ is generated by the Intel timer chip U28 and is connected to U41-1. U41 functions as a 2-to-1 selector/multiplexer. The control signal MCC/$\overline{\text{GEND}}$ from U29-15 controls the selection of the SPOUT or $\overline{\text{GATE END}}$ signals for application to the measurement block. When $\overline{\text{MCC}}$/GEND is high, the $\overline{\text{GATE END}}$ control signal is passed through U41 and inverted by U39C. This output is called the SPMUX signal. When $\overline{\text{MCC}}$/GEND is low, SPOUT will be present at the output of U39C.

5.3.9.2.2 U38B is a D-type flip-flop which controls U28's counters 1 and 2 and their reset and counting function. U38A controls the $\overline{\text{GEND}}$ signal clock via the OUT1 or 2 signal of U28. At the end of each measurement, the $\overline{\text{MLRST}}$ line is brought low, resetting the two internal counters of U28. When the $\overline{\text{MLRST}}$ line goes high, the GATE signal will follow, clocking a high to U38B's Q output allowing U28's two internal counters to begin counting. Once the U38 counter has timed out, the selected OUT signal (1 or 2) will then clock the $\overline{\text{GEND}}$ line high at U38A's Q output.

5.3.9.2.3 Chip U28 is connected to the buffered data bus (BD0-BD7) from U26 of the CPU block. U28 uses two buffered address lines BA1 and BA2 from U27 of the CPU block to address the internal counter and control register. When the gate time is being programmed, the timer chip U28 will receive two to four bytes of data from the microprocessor, depending on the gate time being programmed. Each time a data byte is written into the timer chip, the CSTIMR line is brought low, BA1 and BA2 lines select the internal register, data is placed on the buffered data bus, and the $\overline{\text{PWE}}$ signal clocks the data into the U28 register.

5.3.9.2.4 U28's three counters (0, 1 and 2) have independent clock inputs. Counter 0's clock input (CLKO) is connected to the microprocessor's E clock which runs at 800 kHz. Counter 1's clock input (CLK1) is connected to the 10 MHz reference signal. Counter 2's clock input (CLK2) is connected to the counter 1's OUT1 signal.

5.3.9.2.5 When a new gate time is programmed into U28, the OUT1 and OUT2 signals of U28 are now selected by the microprocessor through U29's LTMS control signal. LTMS is connected to U40B for selecting either U28's OUT1 or OUT2 signal for U38A's clock input. U40B also inverts the OUT1 and OUT2 signal to give U38A a rising edge when U28's signal (OUT1 or OUT2) times out. This inversion is effected because U38 is a positive-edge triggered device and the OUT1 and 2 signals are high-to-low transitions when the programmed gate time has expired.

5.3.9.2.6 LTMS control lines select OUT1 or OUT2 from U28 to pass through U40B to the clock input of U38B. The LTMS control line is set high for programmed times less than 1 millisecond and low for 1 millisecond or greater times. The selected OUT signal passes through U40B to U38A's clock input when the gate counters of U28 time out. This rising edge to U38's clock input clocks the D input to Q output, forcing GEND high. This signals the end of a measurement.

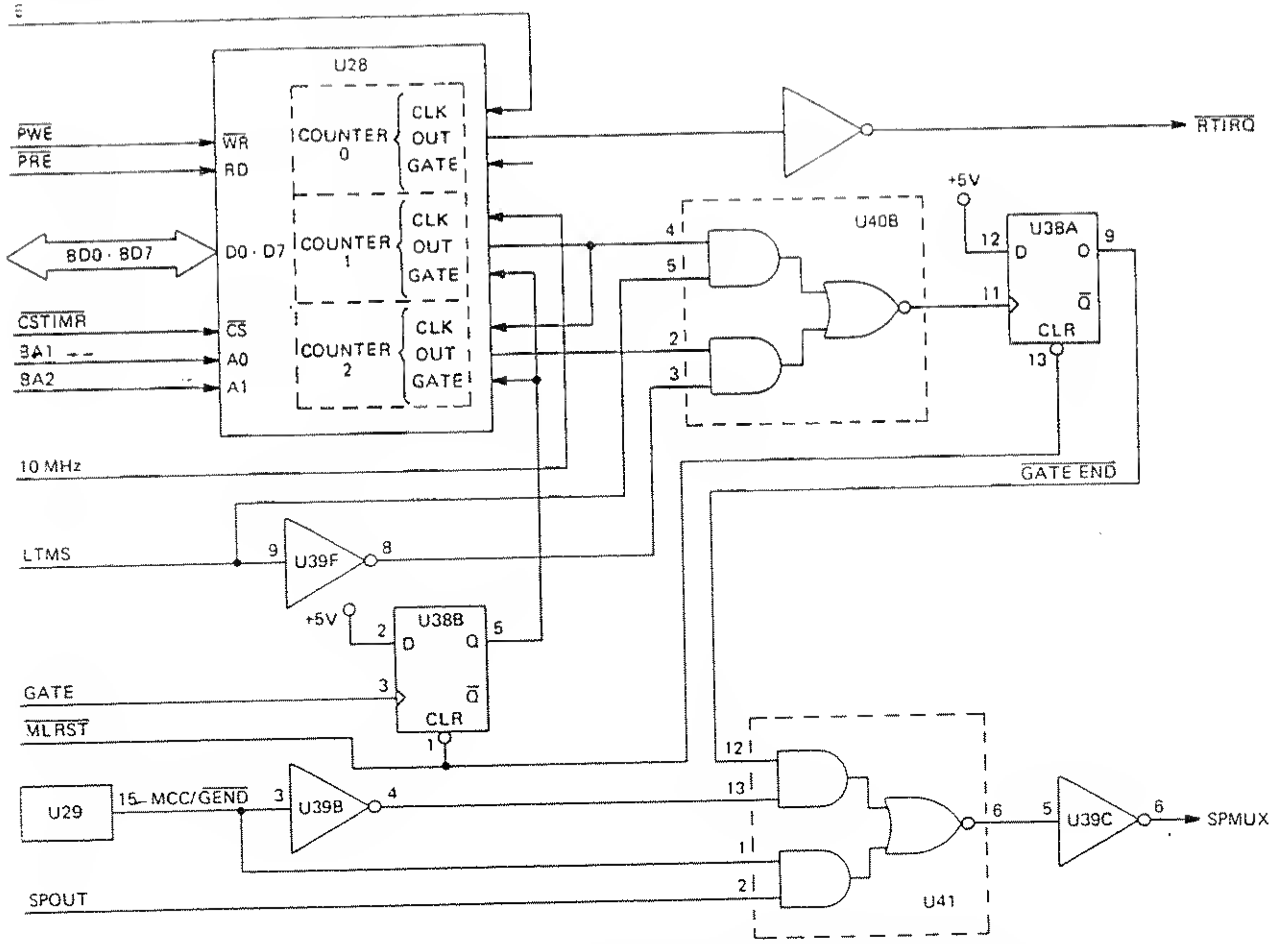


Figure 5.15 - Simplified Schematic for the Internal Gate Timer

5.3.10 External Reference Multiplier Block

5.3.10.1 Functional Description

5.3.10.1.1 Refer to Figure 5.16 which shows a block diagram of the external reference multiplier. The input to the circuit is taken from the REF-IN connector on the instrument's rear panel, via a signal conditioning circuit.

5.3.10.1.2 The circuit contains a 10 MHz oscillator operating in a phase-locked loop. If an external reference signal of suitable amplitude is present at the REF-IN connector, the reference frequency is fed to the external reference detector. The detector output then alerts the CPU through the EXTDET signal that there is an external signal present. The VCO oscillator is then enabled and the INT/EXT logic connects the 10 MHz from the buffer and splitter to the output.

5.3.10.1.3 The pulse generator output is fed to the phase detector, and forms the reference signal for the phase-locked loop. The phase detector is of the sampling type, allowing the oscillator to be phase-locked to a reference signal of 10 MHz or any submultiple of 10 MHz.

5.3.10.1.4- If no external reference signal of suitable amplitude is present at the REF-IN connector, the reference detector output does not trigger the switching signal generator. The oscillator is disabled and the INT/EXT logic connects the internal reference to the measurement logic.

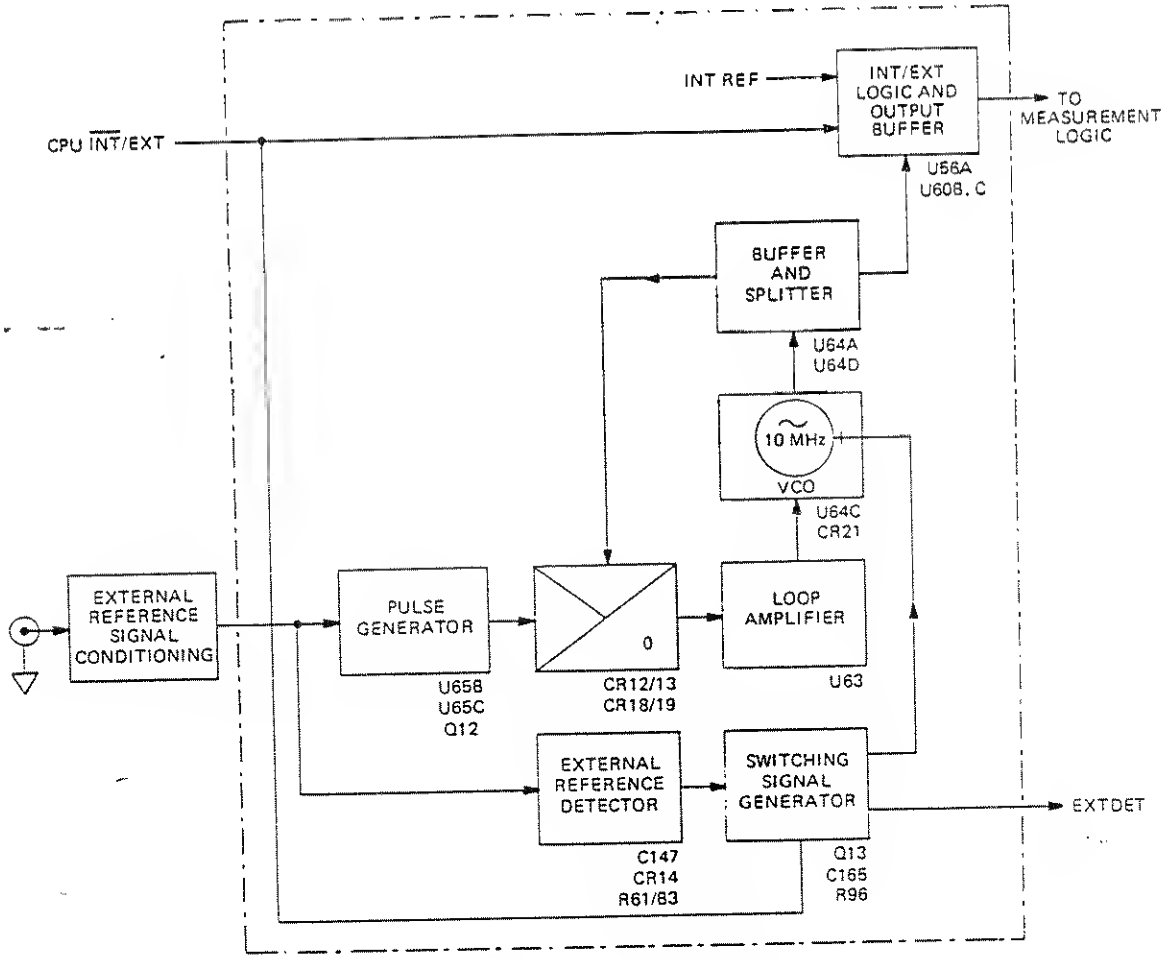


Figure 5.16 - Simplified Diagram for the External Frequency Multiplier Block

5.3.10.2 Circuit Description

5.3.10.2.1 Input Circuit and Pulse Generator

5.3.10.2.1.1 Two antiphase waveforms derived from the external reference signal enter the system at J208 connector. The waveform from J208 is converted to TTL levels by U66 and squared in U65D before being applied to the pulse generator, U65B and U65C. The operation of this circuit is shown in Figure 5.17.

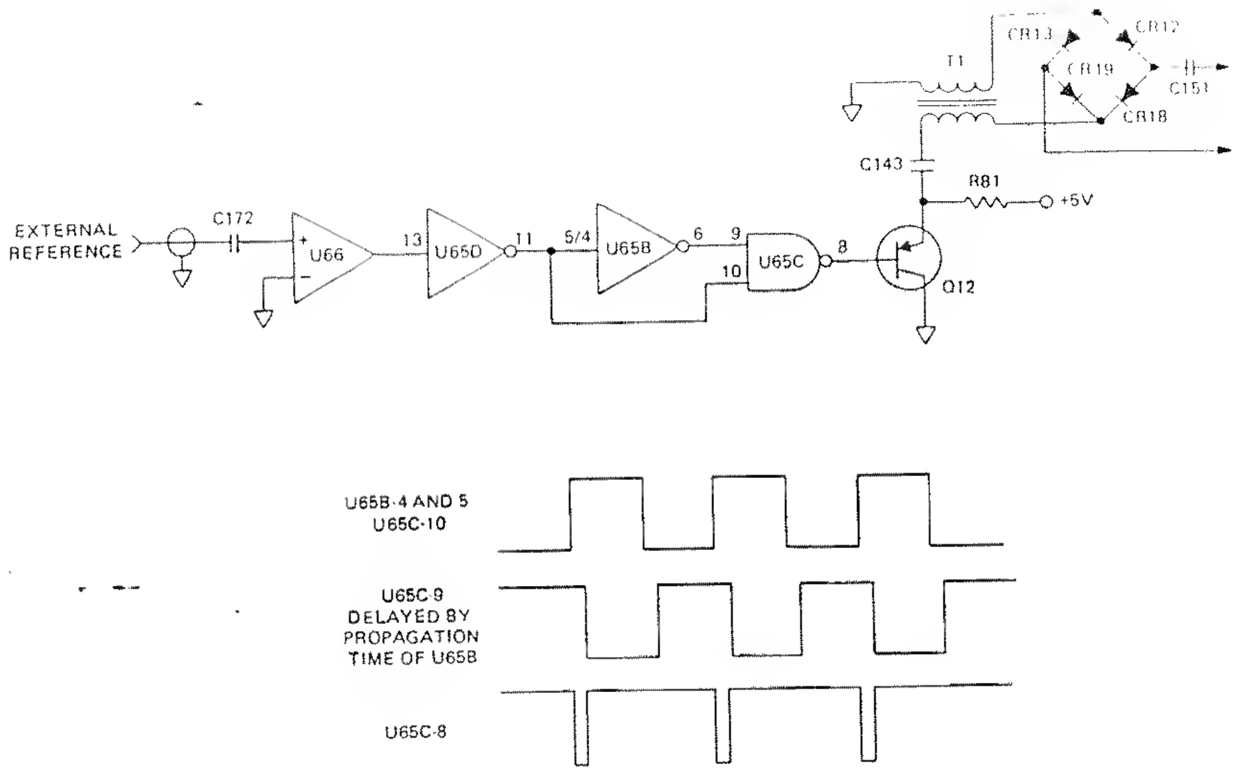


Figure 5.17 - Input Circuit and Pulse Generator

5.3.10.2.1.2 The negative-going pulses at U65-C are used to switch Q12 which drives the transmission-line type transformer T1. The transformer acts as a phase splitter. Thus, for the duration of each pulse from U65C-8, the sampling bridge of the phase detector is held forward-biased, with the CR12/CR13 and CR18/19 junctions symmetrical around 0V.

5.3.10.2.2 Phase-Locked Loop

5.3.10.2.2.1 Refer to Figure 5.17 and 5.18. The loop oscillator's active element is U65C. The oscillator frequency is controlled by the crystal Y1 and the varactor diode CR21. The trimming capacitor C142 can be adjusted to compensate for a range of crystal and varactor tolerances.

5.3.10.2.2.2 The oscillator output drives a unity-gain cascade buffer, U64A/D. The buffered signal from the collector of U64A forms the RF input to the phase detector.

5.3.10.2.2.3 When the sampling bridge of the phase detector is forward-biased by the pulses from T1, the CR18/CR19 junction adopts the same potential as the CR12/CR13 junction. At other times, the junctions are isolated from each other by the high impedance of the non-conducting diodes. The bridge output is therefore a series of samples of the loop oscillator waveform, taken at the frequency of the external frequency standard.

5.3.10.2.2.4 The phase detector output depends upon the relative frequency of the loop oscillator and the frequency standard, and upon the phase of the loop oscillator waveform at the instant of sampling. If the standard frequency is 10 MHz, every cycle of the loop oscillator output is sampled, but if it is a submultiple of 10 MHz, only every second, fourth, fifth, or tenth cycle will be sampled. In all cases, however, provided the standard frequency is an exact submultiple of the loop oscillator frequency, the samples will be of constant amplitude. If the standard frequency is not an exact submultiple of the loop oscillator frequency, the output pulses will be amplitude modulated.

5.3.10.2.2.5 The amplitude of each phase detector output pulse depends upon the instantaneous value of the loop oscillator waveform at the instant of sampling. The pulses are integrated in C144 to form the input to the loop amplifier U63. When the loop is in-lock, the voltage across C144 maintains the voltage at U63-6, and therefore across the varactor, at the level needed to maintain the loop oscillator at the lock frequency.

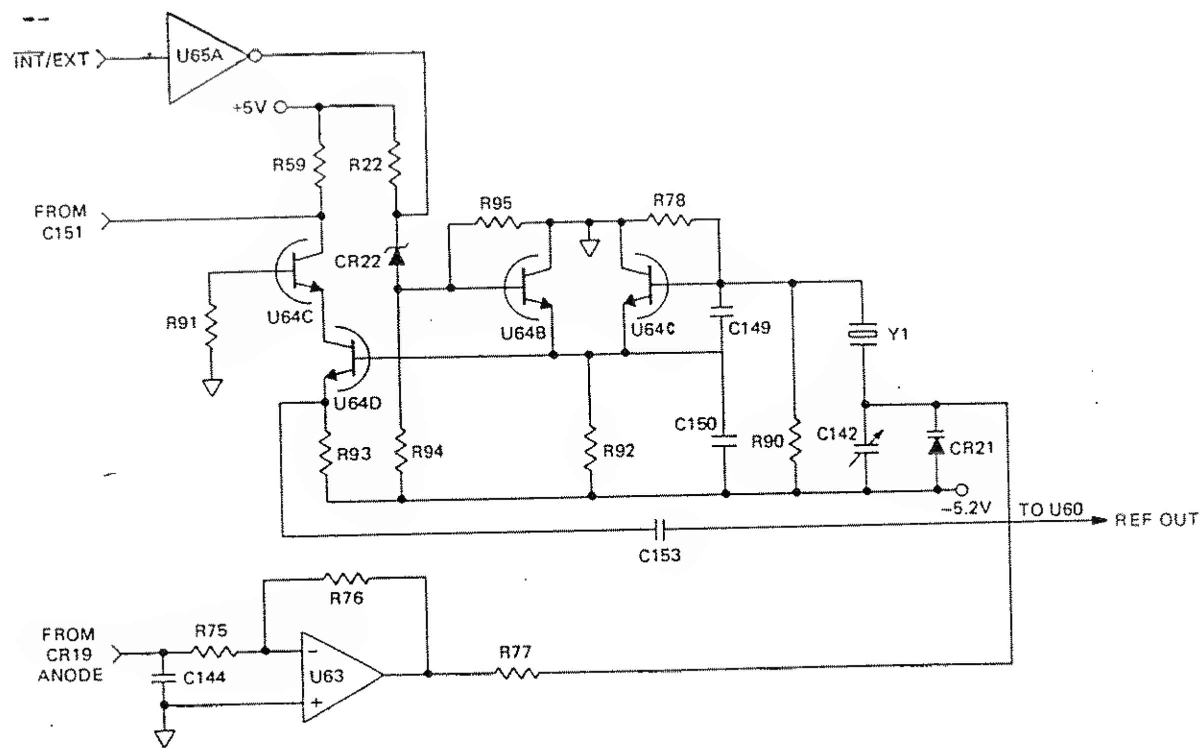


Figure 5.18 - Phase-Locked-Loop Controlled Oscillator

5.3.10.2.3 External Reference Detector and INT/EXT Switching

5.3.10.2.3.1 The output from U65D-11 is fed to a detector formed by C147, CR14, and R61/83. Refer to Figure 5.19. If no external reference signal is present at the REF-IN connector, U66-7 will go high and U65D-11 is at a logic 0. The detector output, and therefore the base of Q13, is at +5V and Q13 is switched off. A logic 0 level is applied to U30-2. When the CPU sees the EXTDET signal low at U30-2, it will, in turn, set U31-6 low (INT/EXT). This is applied to U65A-1, 2 giving a logic 1 at U65A-3. See Figure 5.18.

5.3.10.2.3.2 The zener diode CR22 converts the logic levels from TTL to the level required to switch on U64B. With U64B switched on, the voltage across R92 holds the emitter of U64C positive with respect to its base, disabling the oscillator. With the INT/EXT low at U56A-7, this will deselect the external reference by placing an ECL high at U60B-5 and force any ECL at U60C-10 low. This will now select the internal reference from U60C-14 for the measurement logic. This disables U60B and enables U60C.

5.3.10.2.3.3 When an external reference signal is present at the J208 connector, the output from U65D-11 is a TTL square wave at the external reference frequency. The detector output holds the base of Q13 negative, so that Q13 conducts. Q13's collector is at a logic 1 and its voltage (EXTDET) high. The CPU will detect this and set the INT/EXT signal high. Under these conditions, U64B is cut off and the loop oscillator is enabled.

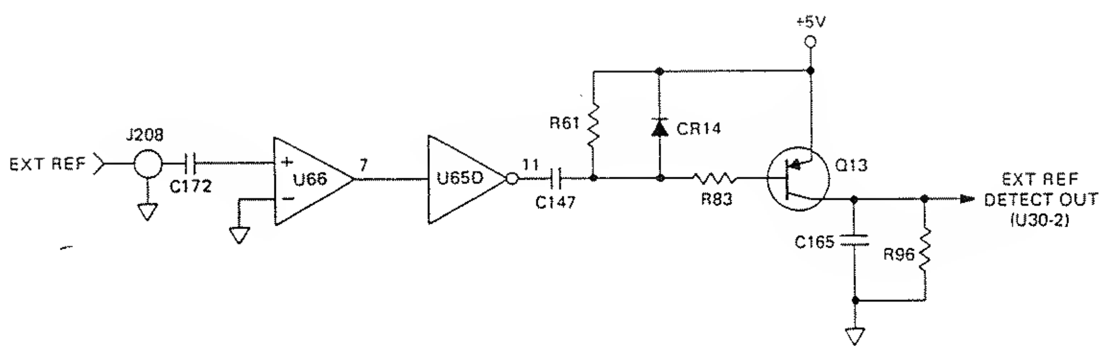


Figure 5.19 - External Reference Detector

5.3.11 Channel D Block

5.3.11.1 Refer to Figure 5.20. Channel D conditioning circuitry provides input signal limiting/buffering with threshold selection of 0V or 1.25V for AC or TTL channel D input compatibility. Resistors R63 and R99 form a 4:5 DC divider with C163 allowing fast edges to pass through to U62. CR24 and CR25 act as clamps, limiting signal swing from -2.5V to +2.3V.

5.3.11.2 The signal then is fed to voltage comparator U62. The output of U62 will change states when the input crosses the reference voltage on pin 3 of U62. The reference voltage can assume one of two possible levels, 0V or 1.25V. When a TTL logic 0 is applied to the base of Q16, Q16 turns on.

5.3.11.3 Resistors R67 and R100 form a 1:4 voltage divider. The voltage divider then applies a 1.25V reference signal to U62 via resistor R101. When a logic 1 is applied to Q16, Q16 turns off. The reference voltage becomes 0V. Resistor R102 provides positive feedback creating a small amount of hysteresis.

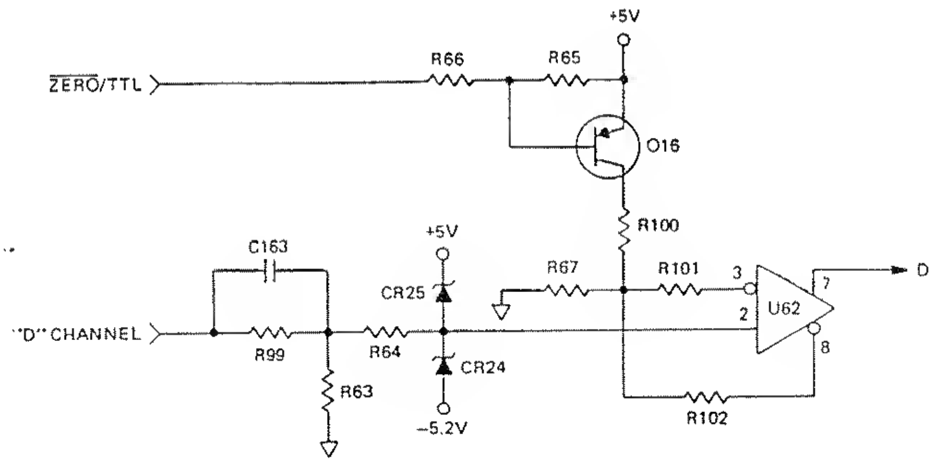


Figure 5.20 - Simplified Block Diagram for Channel D

5.3.12 GPIB Block

5.3.12.1 Functional Description

5.3.12.1.1 Refer to Figure 5.21. The GPIB block for the 1995/1996 consists of only three chips. These include the general interface bus controller (Texas Instruments TMS9914A) and two bus transceivers (75160 and 75161). These provide the necessary interface between the IEEE-bus and the GPIB controller.

5.3.12.1.2 U61 (TMS9914A) is used when it is necessary for an intelligent instrument to communicate with an IEEE-488 General Purpose Interface Bus (GPIB). It performs the interface function between the microprocessor and the bus, relieving the microprocessor of the task of maintaining IEEE protocol. By utilizing the interrupt capabilities of the bus controller U61, the bus does not have to be continually polled, and rapid responses to changes in the interface configuration can be achieved.

5.3.12.1.3 U61 provides an interface between the microprocessor and the GPIB as specified in the IEEE-488 Standard. This device is controlled and configured through 8-bit memory-mapped registers and enables all aspects of the Standard to be implemented, including talker, listener and controller.

5.3.12.1.4 Refer as required to Figure 5.21 which provides a block diagram showing the interfacing of the microprocessor and the GPIB block.

5.3.12.2 Circuit Description

5.3.12.2.1 The input/output pins (DI01 through DI08) of U61 are connected to the IEEE-488 bus via bus transceivers U67 and U68. The direction of data flow is controlled by the TE and $\overline{\text{CONT}}$ output signals generated by U61.

5.3.12.2.2 Communication between the microprocessor and U61 is performed via memory-mapped registers. There are 13 registers within U61, six of which are read registers and seven are write registers. These registers are used to both pass control data to and get status information from the microprocessor.

5.3.12.2.3 The least significant address (BA1, BA2 and BA3) lines from the address buffer U27 are connected to the register select lines RS0, RS1 and RS2. These latter lines determine the particular register selected. When U61's $\overline{\text{CE}}$ input is pulled low by the $\overline{\text{CSGPIB}}$ control line, any one of the eight consecutive addresses is selected. Reading and writing to these locations transfers information between U61 and the microprocessor.

5.3.12.2.4 U67 is a 20-pin device used to buffer the IEEE-488 data lines (DI01 through DI08) in all applications. The direction of the buffers is controlled by the Talk-Enable (TE) output of U61. This active high signal becomes true whenever U61 is in TACS (addressed to talk) or SPAS (serial polled) mode.

5.3.12.2.5 U68 is a 20-pin device used to buffer the IEEE-488 measurement lines. It may be used for talker or listener status. The direction of the handshake-line buffers NRFD, NDAC and DAV are again controlled by the TE signal from U61. However, the SRQ, ATN, REN and IFC buffers are controlled by the DC input of U68. U68 connects with the Controller Active ($\overline{\text{CONT}}$) output of U61. The $\overline{\text{CONT}}$ output always remains high because U61 is not being used as a controller device. U68 also includes the logic necessary to control the direction of the EOI buffer. This is dependent on the TE signal when ATN is false (high) and on the DC signal when ATN is true (low).

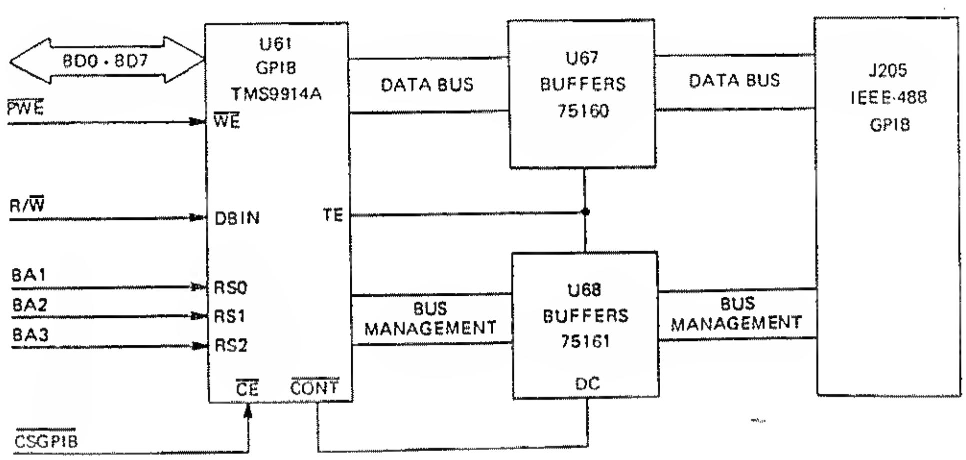


Figure 5.21 - Simplified Diagram for the GPIB Block

6.1 INTRODUCTION

6.1.1 The performance tests in this section are used for (1) receiving inspection/acceptance, (2) periodic determination of the need for recalibration, (3) upon failure of a routine specification check, and (4) after repair of unit. Verify the basic operation of the counter before starting these tests by completing the rapid functional check found in Subsection 2.9.

6.1.2 Satisfactory completion of these performance tests will confirm the 1995/1996's operation by measurement function. Instrument covers need not be removed for any test. Complete the performance tests in the order given.

6.1.3 The following conditions must be maintained during these tests:

a. The counter must be operated from an AC supply

b. The line voltage must be within ± 10% of the indicated value of the line voltage selector

c. The ambient temperature must be 23°C ± 2°C

d. The power supply to the internal frequency standard must remain uninterrupted. (This does not apply if the counter is locked to an external frequency standard.)

6.1.4 Warm up the counter for one hour (switched to standby if necessary) before beginning these tests.

6.2 REQUIRED TEST EQUIPMENT

6.2.1 Table 6.1 lists the necessary test equipment for these performance tests. Equipment having operating characteristics equivalent to or better than those listed may be substituted. The procedures described in this section are general in nature and based on the use of the test equipment recommended. Some modification of the procedures may be required if substituted equipment is used.

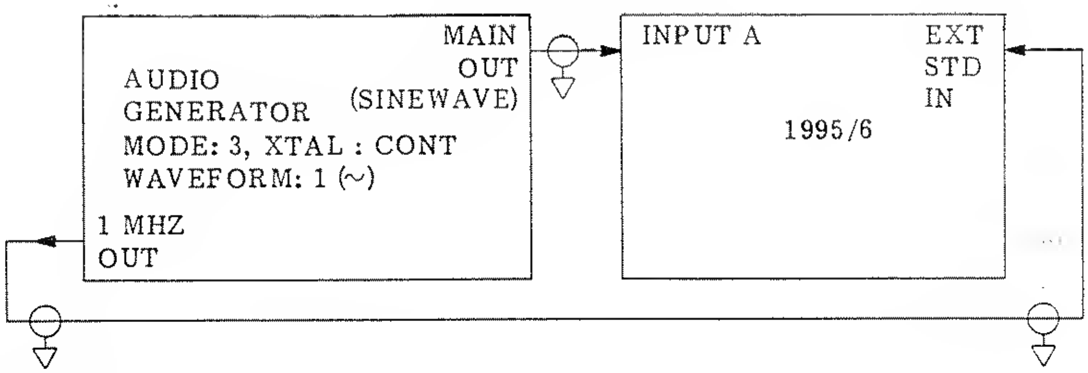
Table 6.1 - Required Test Equipment

	Item	Minimum Use Specifications	Quantity	Recommended Equipment
1.	Signal Generator	10 kHz to 1.3 GHz amplitude 5 mV rms to 1V rms into 50 ohms. 1 kHz AF out	1	Racal-Dana Model 9087
2.	Audio Generator	10 Hz to 10 kHz; amplitude of 25 mV rms into 50 ohms	1	Racal-Dana Model 845
3.	AC Voltmeter (low frequency)	DC to 10 kHz; .1% resolution, and ± 2.5% accuracy	1	Racal-Dana Model 5002
4.	Pulse Generator	1 Hz to 5 MHz, external lock and trigger capability; ± 2 ns jitter	1	Racal-Dana Model 1500
5.	AC Voltmeter (high frequency)	10 kHz to 2 GHz; .1% resolution,and ± 2.6% accuracy to 500 MHz & ± 5% accuracy to 1.3 GHz	1	Racal-Dana Model 9303
6.	BNC T-Connector	50 Ohms	1	—
7.	Connector Lead	50-ohm coaxial cable with BNC connectors, ≈ 4 ft. long	5	—
8.	Coaxial Load	BNC connector, 50 ohms, 2W BNC ± 1%	1	—
9.	N-type to BNC adapter/connector	50 ohm	1	—

Table 6.4 - Input A Sensitivity Performance Test, II

Applied Frequency : Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
20 Hz	25 mV rms	± .1 Hz	100-ms gate	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   FREQ A
   Input A 50-ohms input impedance
   Gate time 0.1 sec
   Disable input A auto trigger
   Set input A trigger level to 0.00V

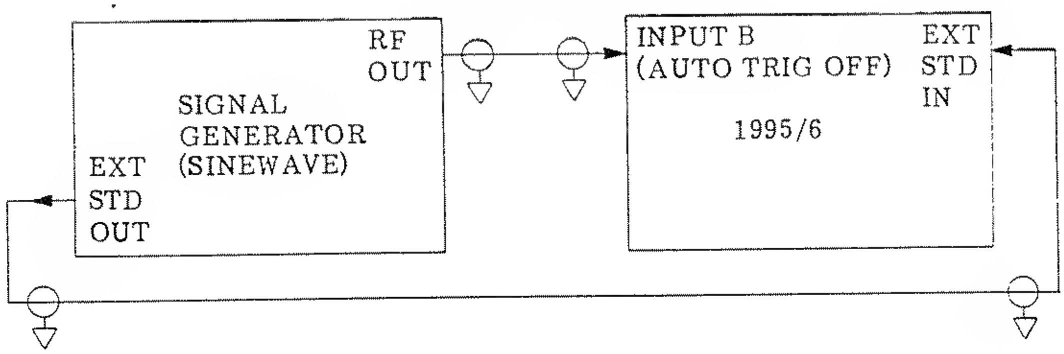
3. Connect the 1995/6 and audio generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

Table 6.5 - Input B Sensitivity Performance Test, I

Applied Frequency	Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
200 MHz		50.0 mV rms	± .2 Hz	1-sec gate	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT
100 MHz		25.0 mV rms	± .1 Hz	1-sec gate	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   FREQ A
   Enable Special Function 21
   Input B 50-ohms input impedance
   Gate time 1 sec
   Input B attenuation to X1
   Set input B trigger level to 0.00V

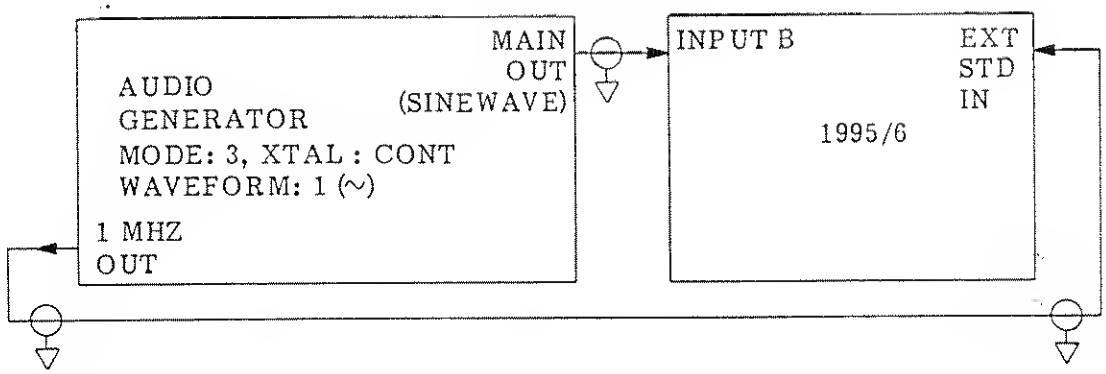
3. Connect the 1995/6 and signal generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

Table 6.6 - Input B Sensitivity Performance Test, II

Applied Frequency : Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
20 Hz	25 mV rms	± .1 Hz	100 ms gate	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   FREQ A
   Enable Special Function 21
   Input B 50-ohms input impedance
   Gate time 0.1 sec
   Input B attenuation to X1
   Set input B trigger level to 0.00V

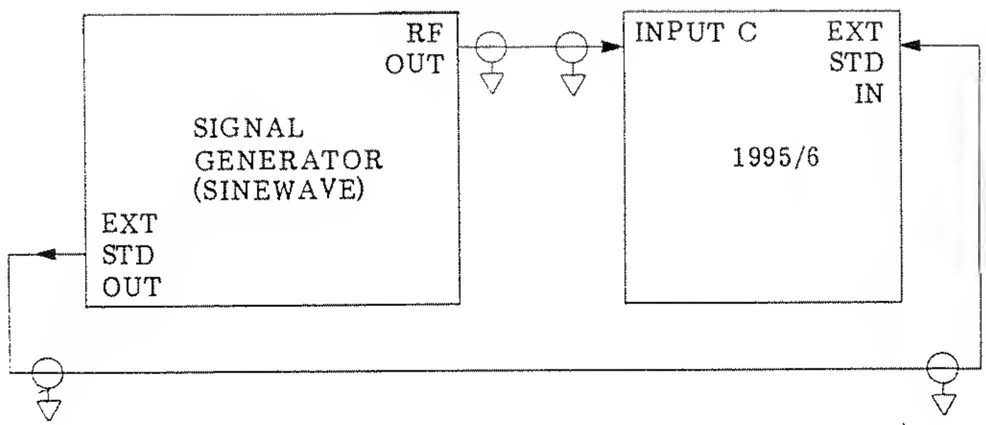
3. Connect the 1995/6 and audio generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

Table 6.7 - Input C Sensitivity Performance Test (1996)

Applied Frequency : Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
1.3 GHz 1.0 GHz 40 MHz	50 mV rms 10 mV rms 10 mV rms (7V max)	± 2 Hz ± 1 Hz ± .1 Hz	1-sec gate 1-sec gate 1-sec gate	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: FREQ C
   Gate time 1 sec

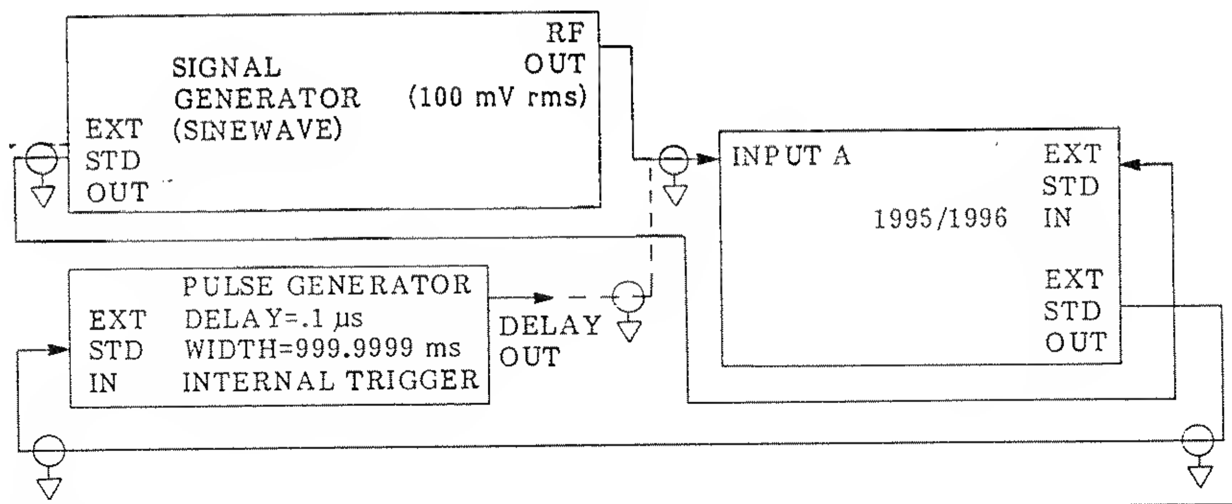
3. Connect the 1995/6 and signal generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

Table 6.8 - Period A Performance Test

Applied Frequency : Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
200 MHz/5 ns 1 Hz/1s	100 mV rms TTL into 50	$\pm 1 \times 10^{-17}$ sec $\pm 1 \times 10^{-9}$ sec	1-sec gate 1-sec gate	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   PERIOD A
   Input A 50-ohms input impedance
   Input A DC coupled
   Gate time 1 sec
   Disable input A auto trigger
   Set input A trigger level to 0.00V

3. Connect the 1995/6 and signal generator as shown above.

4. Apply 200 MHz, 100 mV rms to input A of the 1995/6 and verify that the measurement taken is within the specified tolerance.

5. Disconnect the signal generator and connect the pulse generator DELAY OUT to input A of the 1995/6. Set the pulse generator to a delay of 0.1 microsec. and width 999.9999 msec.

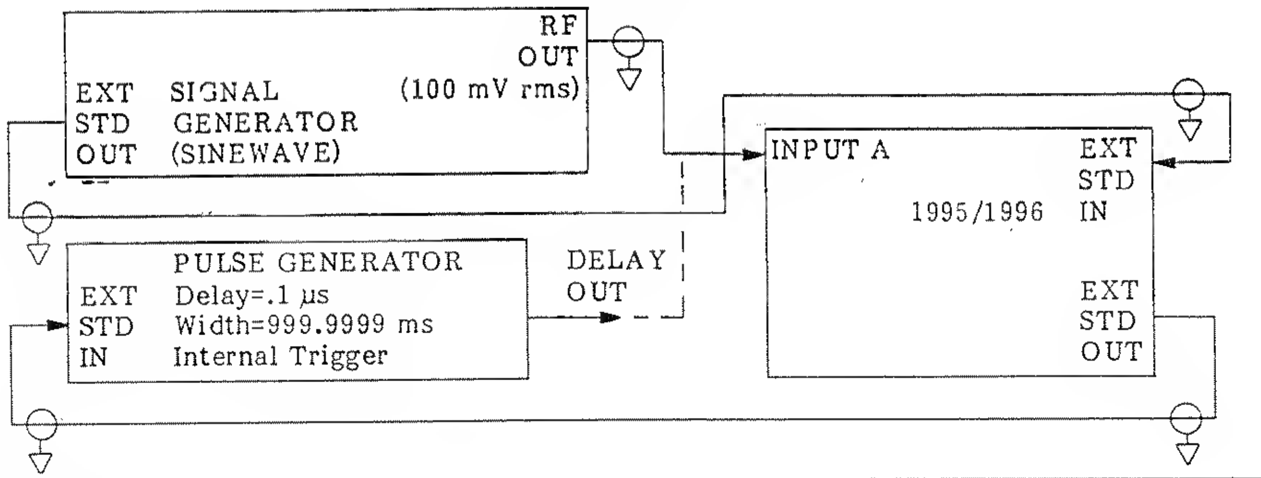
6. Set the 1995/6 to input A trigger level of 1.30V.

7. Verify that the measurement is within the specified tolerance.

Table 6.9 - Time Interval A→B Performance Test

Applied Frequency : Performance Standard	Required Input Signal	Tolerance	Special Notes
100 MHz/5 ns 1 Hz/1s	100 mV rms TTL into 50Ω	± 3 ns ± 3 ns	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: TI A→B
   Input A 50-ohms input impedance
   Input A DC coupled
   Disable input A auto trigger
   Set input A trigger level to 0.00V
   Enable COM A

3. Connect the 1995/6 and signal generator as shown above.

4. Apply 100 MHz, 100 mV rms to input A of the 1995/6.

5. Verify that the measurement is within the tolerance specified above.

6. Set the 1995/6 to Slope A˥, Slope Bʃ.

7. Verify that the measurement is within the tolerance specified above.

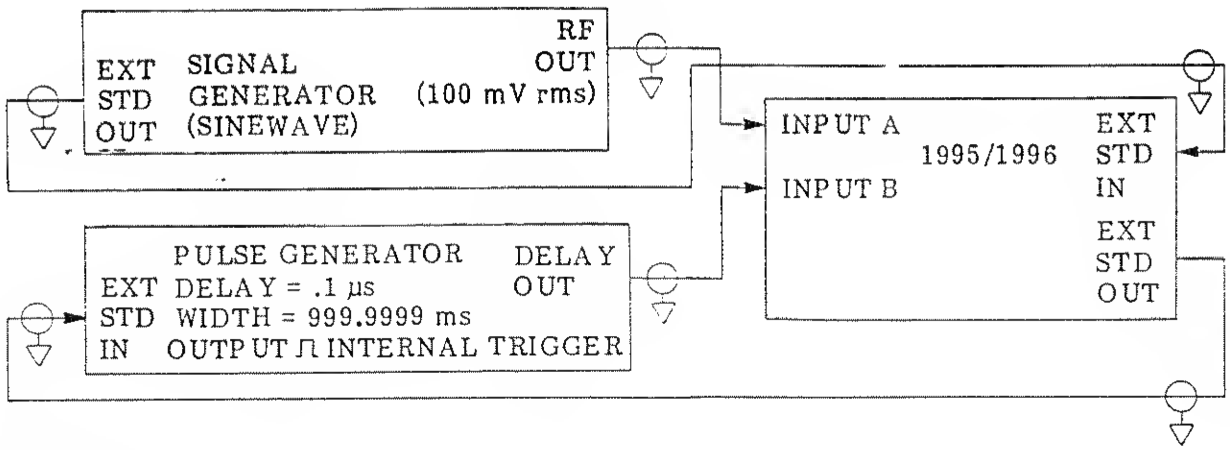
Table 6.9 - Time Interval A→B Performance Test (Cont'd)

PROCEDURE
8. Disconnect the signal generator and connect the pulse generator DELAY OUT to input A of the 1995/6. Set the pulse generator to a delay of 0.1 microsec., width 999.9999 msec., INT trigger.
9. Set the 1995/6 inputs A and B trigger levels to 1.30V.
10. Set inputs A and B to Slope ∫.
11. Set the 1995/6 DELAY to 1 msec and enable the DELAY.
12. Verify that the measurement is within the tolerance specified above.

Table 6.10 - Total A by B Performance Test

Applied Frequency: A	B	Number of Counts	Tolerance	Special Notes
100 MHz	.9999999 Hz	99.99999×10^6	± 1 count	
20 kHz	10 kHz	1	± 1 count	

Test Setup



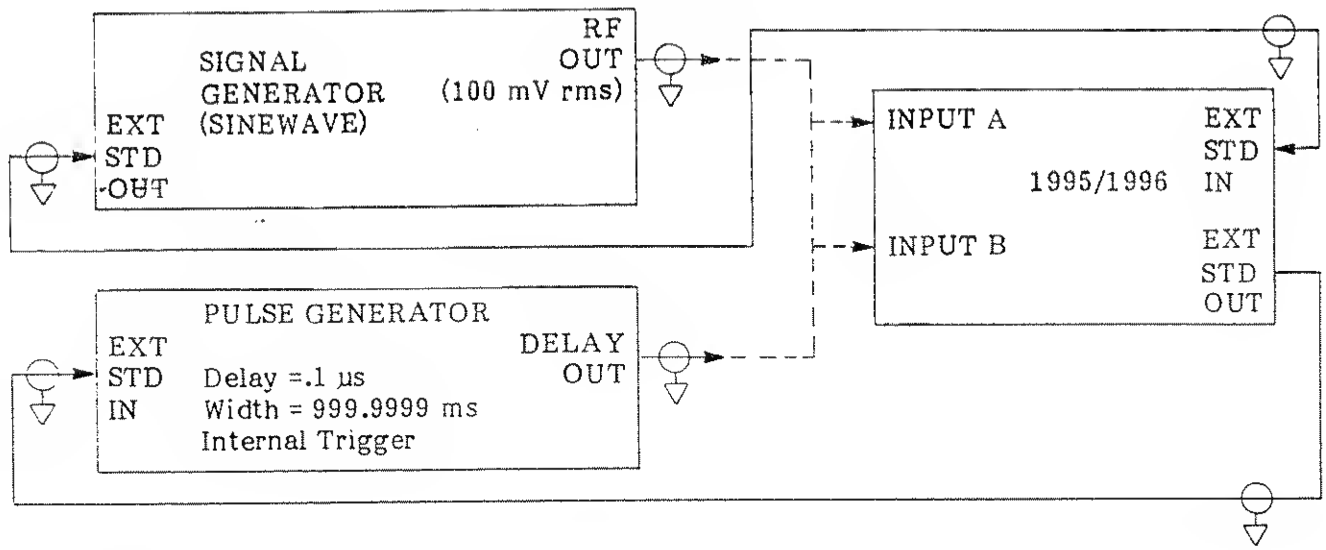
PROCEDURE

1. Power up the 1995/6.
2. Set the 1995/6 as follows:
   - TOTAL A by B
   - Input A 50 ohms input impedance
   - Input B 50 ohms input impedance
   - Input A DC coupled
   - Input B DC coupled
   - Disable input A auto trigger
   - Set input B attenuation to X1
   - Set input A trigger level to 0.00V
   - Set input B trigger level to 1.30V
   - Select slope ⨍ for input B
3. Connect the 1995/6 to the signal generator and pulse generator as shown above.
4. Set the signal generator to an output of 100 MHz, 100 mV rms.
5. Set the pulse generator to an output of 0.1 microsec. delay and width 999.9999 msec.
6. Verify that the measurement is within the tolerance specified above.
7. Set the signal generator to an output of 20 kHz, 100 mV rms.
8. Set the pulse generator to an output of 50 microsec. delay and width 50 microsec.
9. Verify that the measurement is within the tolerance specified above.

Table 6.11 - Ratio A/B Performance Test

Applied Frequency: A	B	Performance Standard	Tolerance	Counter Resolution	Special Notes
200 MHz	1 Hz	200.0000000×10^6	± 1 count	1-sec gate	
1 Hz	—	1.000000000	± 1 count		

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   RATIO A/B
   Input A 50 ohms input impedance
   Input B 50 ohms input impedance
   Input A DC coupled
   Input B DC coupled
   Disable input A auto trigger
   Set input B attenuation to X1
   Set input A trigger level to 0.00V
   Set input B trigger level to 1.30V
   Gate time 1 sec.

3. Connect the 1995/6 to the signal generator and pulse generator as shown above.

4. Set the signal generator to an output of 200 MHz, 100 mV rms.

5. Set the pulse generator to an output of 0.1 microsec. delay and width 999.9999 msec.

6. Verify that the measurement is within the tolerance specified above.

7. Disconnect the signal generator from input A. Transfer the pulse generator output from input B to input A.

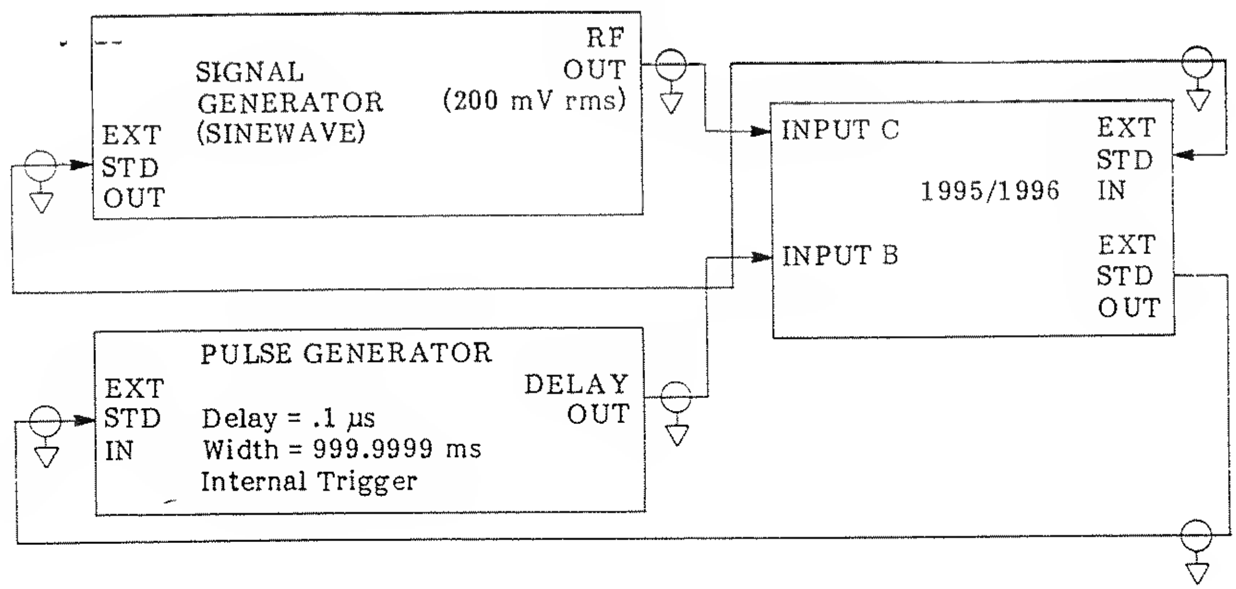
8. Enable COM A on the 1995/6 and set input A trigger level to 1.30V.

9. Verify that the measurement is within the tolerance specified above.

Table 6.12 - Ratio C/B Performance Test

Applied Frequency: C	B	Performance Standard	Tolerance	Counter Resolution	Special Notes
1.3 GHz	1 Hz	1.30000000×10^9	± 2 count	1-sec gate	
40 MHz	1 Hz	40.0000000×10^6	± 2 count	1-sec gate	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows:
   RATIO C/B
   Input B 50 ohms input impedance
   Input B DC coupled
   Set input B attenuation to X1
   Set input B trigger level to 1.30V
   Gate time 1 sec

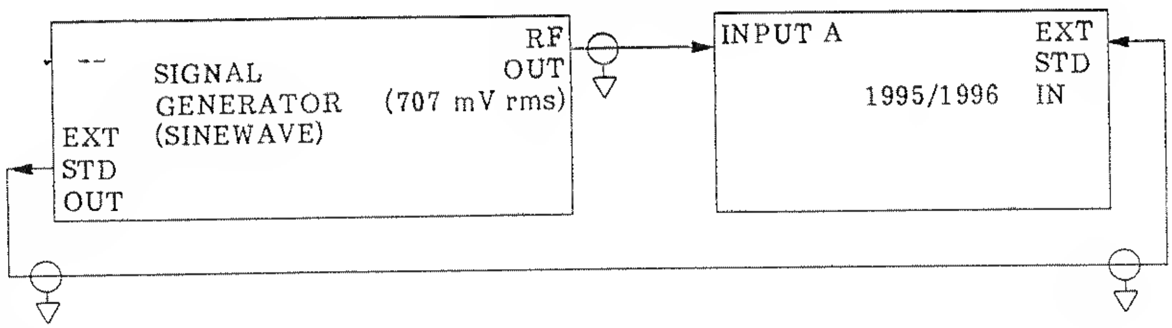
3. Connect the 1995/6 to the signal generator and pulse generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

Table 6.13 - Rise Time A Performance Test

Applied Frequency : Performance Standard	Tolerance	Special Notes
50 MHz/6.0 ns	± 3ns	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

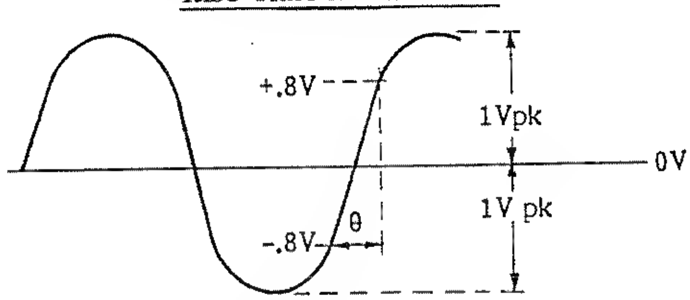
Test Setup



PROCEDURE

1. Power up the 1995/6.
2. Set the 1995/6 as follows: RISE A
   Input A 50 ohms input impedance
3. Connect the 1995/6 to the signal generator as shown above.
4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Rise Time A Waveform

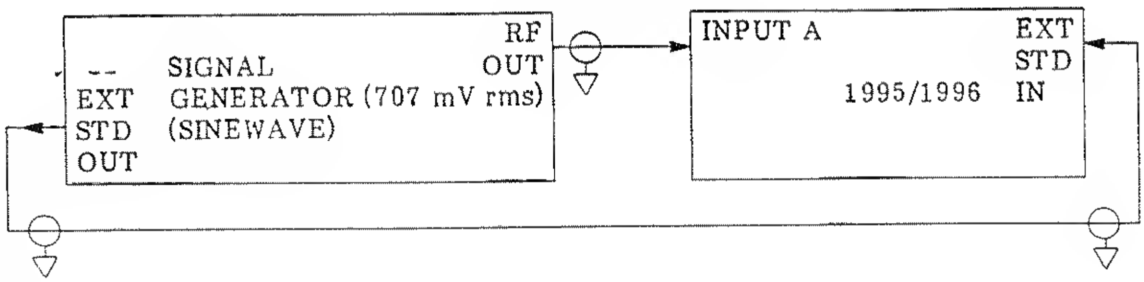


$$\text{Rise Time} = \frac{.3}{50 \times 10^6} = 6 \text{ ns}$$

Table 6.14 - Fall Time A Performance Test

Applied Frequency : Performance Standard	Tolerance	Special Notes
50 MHz/6.0 ns	± 3 ns	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

Test Setup



PROCEDURE

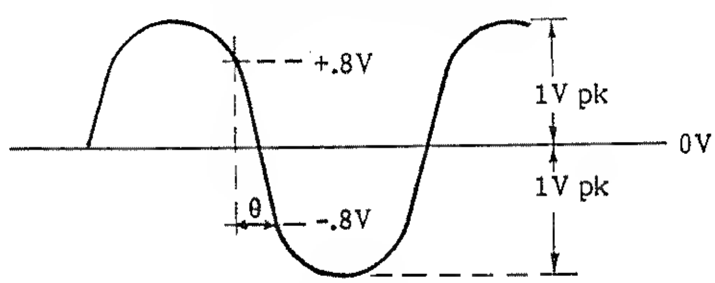
1. Power up the 1995/6.

2. Set the 1995/6 as follows: FALL A
   Input A 50 ohms input impedance

3. Connect the 1995/6 to the signal generator as shown above.

4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Fall Time A Waveform

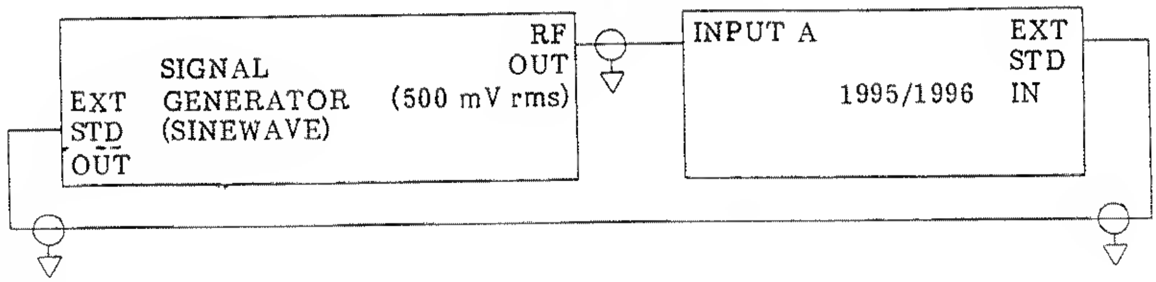


$$\text{Fall Time} = \frac{.3}{50 \times 10^6} = 6.0 \text{ ns}$$

Table 6.15 - Positive Pulse Width Performance Test

Applied Frequency : Performance Standard	Tolerance	Special Notes
100 MHz/5 ns	± 3 ns	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: POS WIDTH A
   Input A 50 ohms input impedance

3. Connect the 1996 to the signal generator as shown above.

4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Positive Pulse Width Waveform

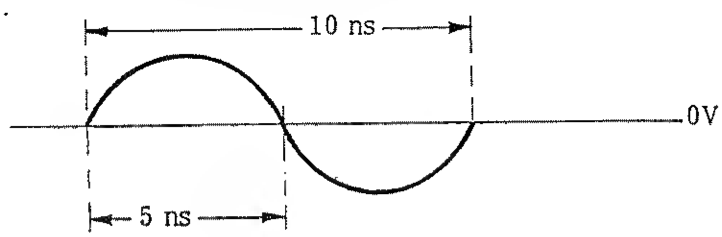
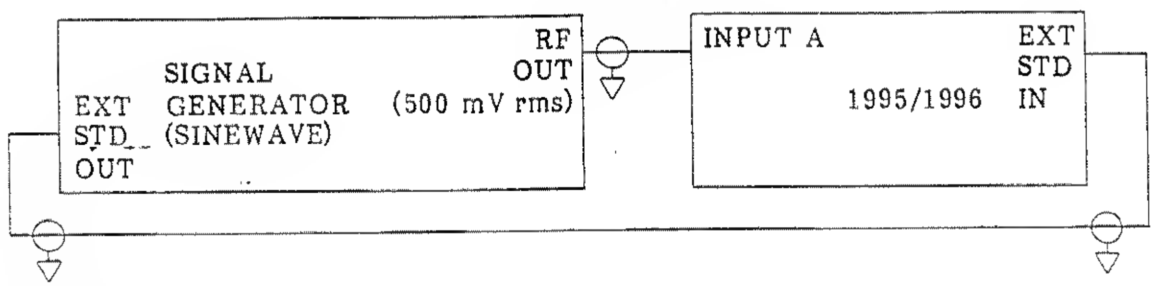


Table 6.16 - Negative Pulse Width Performance Test

Applied Frequency : Performance Standard	Tolerance	Special Notes
100 MHz/5 ns	± 3 ns	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: NEG WIDTH A
   Input A 50 ohms input impedance

3. Connect the 1996 to the signal generator as shown above.

4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Negative Pulse Width Waveform

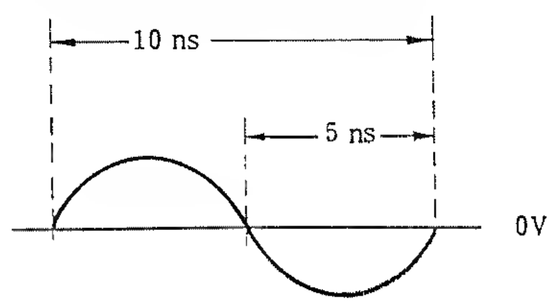
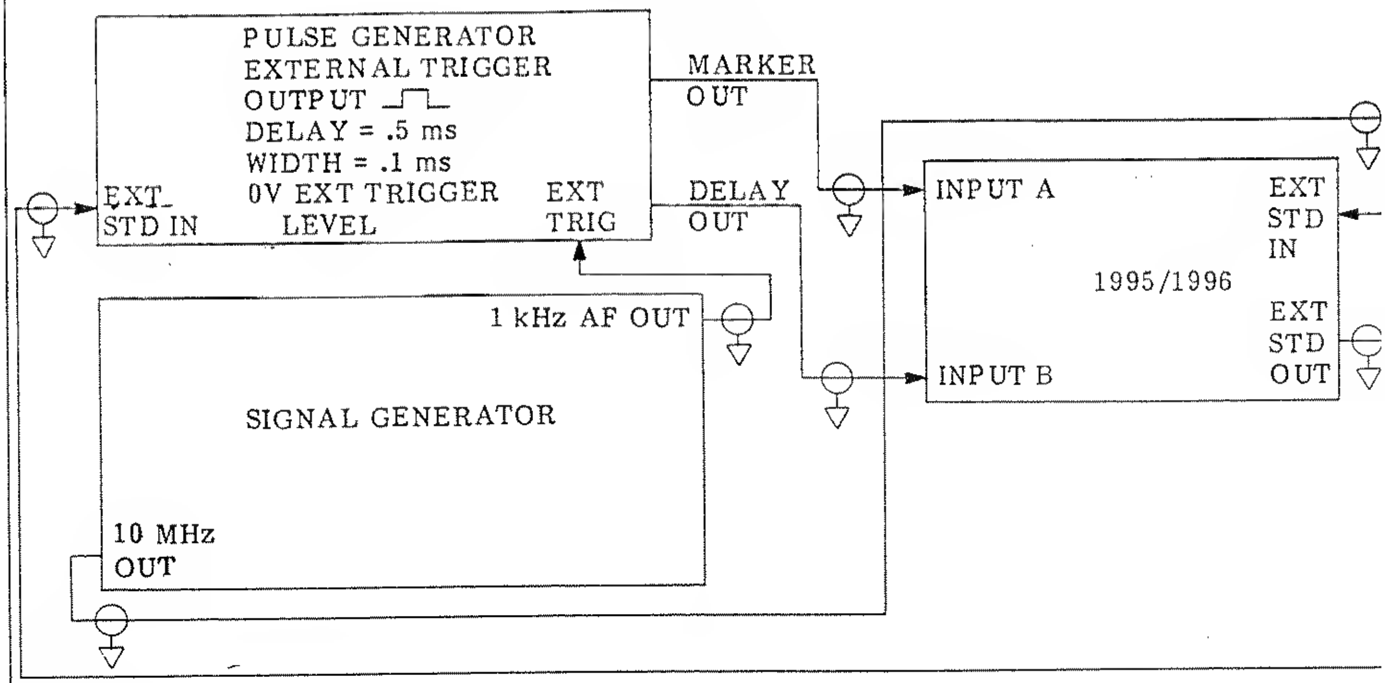


Table 6.17 - Phase A rel B Performance Test

Applied Frequency	Performance Standard	Tolerance	Counter Resolution	Special Notes
1 kHz	180^{o}	$\pm .1^{o}$	1-sec gate	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: PHASE A REL B
   Input A 50 ohms input impedance
   Input B 50 ohms input impedance
   Gate time 1 sec

3. Connect the 1996 to the signal generator and pulse generator as shown above.

4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Phase A rel B Waveform

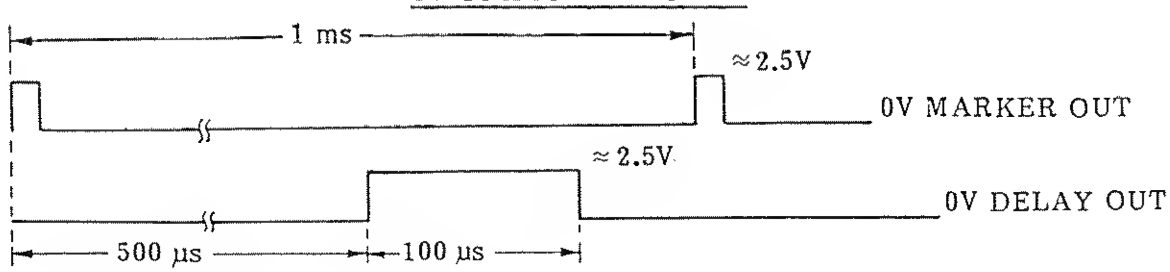
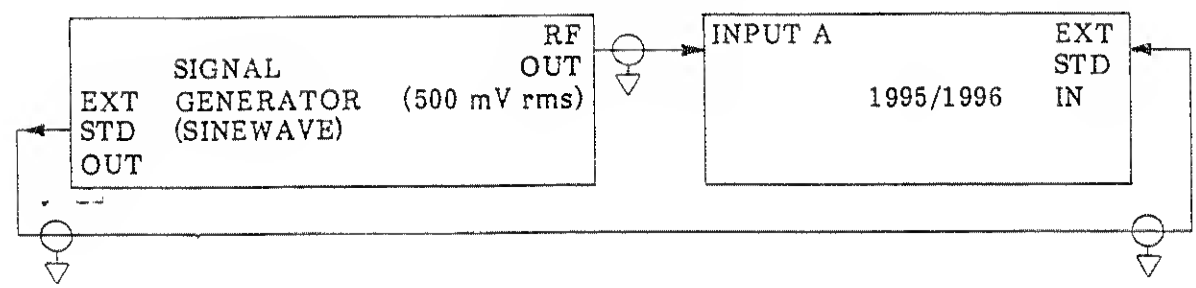


Table 6.18 - Duty Cycle A Performance Test

Applied Frequency	Performance Standard	Tolerance	Special Notes
10 MHz	50%	± 4%	

Test Setup



PROCEDURE

1. Power up the 1995/6.

2. Set the 1995/6 as follows: DUTY A
   Input A 50 ohms input impedance

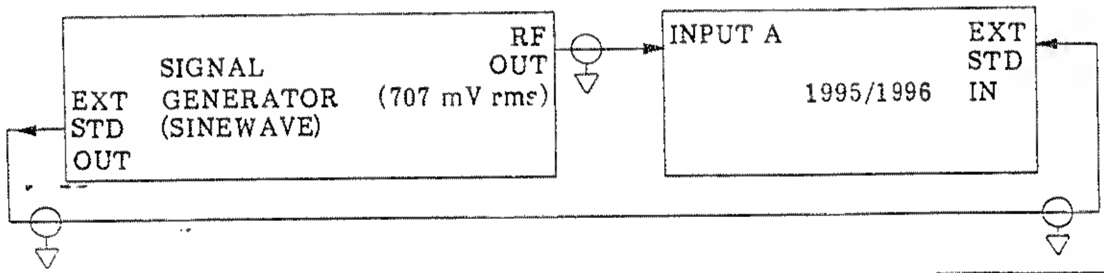
3. Connect the 1996 to the signal generator as shown above.

4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Table 6.19 - Slew Rate A Performance Test

Applied Frequency : Performance Standard	Tolerance	Special Notes
5 MHz/29 x 10^6V/s	± 6 x 10^6V/s	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

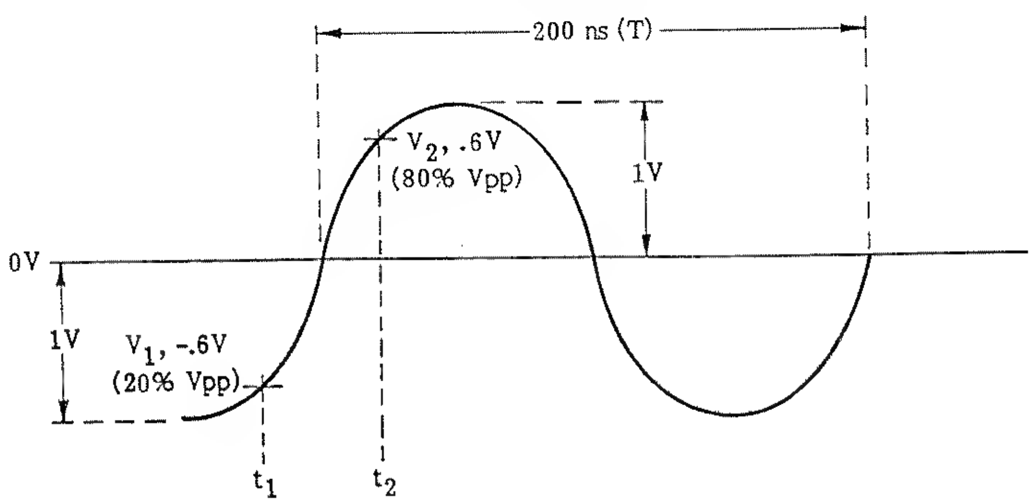
Test Setup



PROCEDURE

1. Power up the 1995/6.
2. Set the 1995/6 as follows: SLEW A
   Input A 50 ohms input impedance
3. Connect the 1996 to the signal generator as shown above.
4. Apply the input shown in the table above and verify that the measurement taken is within the specified tolerance.

Slew Rate A Waveform



$$\text{Slew Rate} = \left(\frac{V_2 - V_1}{t_2 - t_1}\right) = \frac{1.2\text{V}}{40.96 \times 10^{-9}\text{ sec}} \simeq \frac{29.3 \times 10^6\text{V}}{\text{Sec}}$$

$$V_2 - V_1 = .6 - (-.6) = 1.2\text{V}$$

$$t_2 - t_1 = \frac{2\,(\text{SIN}^{-1}\ .6)}{360} \times T = \frac{73.74^\circ}{360^\circ} \times 200\text{ ns} = 40.96\text{ ns}$$

6.4 CALIBRATION

6.4.1 This procedure provides calibration information for Racal-Dana's Universal Systems Counters Models 1995/1996.

6.5 REQUIRED EQUIPMENT FOR CALIBRATION

a. Digital voltmeter with at least a 1 mV accuracy in the 10V range. Use a Racal-Dana Model 5004 or its equivalent

b. GPIB controller. Use a Hewlett-Packard Model 9826 or its equivalent

c. DC source with a single-pole output filter set for a 3-dB cutoff frequency of 1.6 Hz (1 KΩ resistor and 100 μF capacitor)

6.6 CALIBRATION PROCEDURE

a. Turn unit-under-test (UUT) on. Allow 15 minutes for thermal stabilization of the counter

b. Send the following string to the counter:

"CAL" <cr lf>

The counter now enters the calibration routine.

NOTE:

If at any point during the calibration procedure an error is generated (e.g., syntax or calibration), the entire calibration procedure must be repeated.

c. Send the following string to the counter:

"CLHI" <cr lf>

d. Connect the voltmeter to the Start DAC (START-CAL LEVEL) output on the rear panel of the UUT and record this voltage (Vstart-high)

e. Connect the voltmeter to the Stop DAC (STOP-CAL LEVEL) output on the rear panel of the UUT and record this voltage (Vstop-high)

f. Send the following string to the counter:

"CLLO" <cr lf>

g. Record the voltage reading of the meter at the Stop DAC (STOP-CAL LEVEL) output of the UUT (Vstop-low)

h. Connect the voltmeter to the Start DAC (START-CAL LEVEL) output of the UUT and record this voltage (Vstart-low)

i. Send the following string to the counter:

"CLTH<space> Vstart-high" <cr lf>
"CLPH<space> Vstop-high" <cr lf>
"CLTL<space> Vstart-low" <cr lf>
"CLPL<space> Vstop-low" <cr lf>

where Vstart-high, Vstop-high, Vstart-low, and Vstop-low are the previously recorded values. At this point "CAL" is shown on the main display. The following example shows the command strings to be sent with a Model HP85B controller in performing a 1995/1996 calibration procedure:

Output703;"CAL"
Output703;"CLHI" (Record Vstart-high and Vstop-high)
Output703;"CLLO" (Record Vstart-low and Vstop-low)
Output703;"CLTH<space>5.2664" (5.2664 is Vstart-high)
Output703;"CLPH<space> 5.2884" (5.2884 is Vstop-high)
Output703;"CLTL<space>-5.2756" (-5.2756 is Vstart-low)
Output703;"CLPL<space>-5.2661" (-5.2661 is Vstop-low)

NOTE:

Header separators, typically commas or semicolons, are controller-dependent.

j. About 5 minutes later, when calibration is completed, "CAL donE" is displayed on the front panel. Values can now be stored to non-vol memory. Depress the calibration switch (through the front-panel opening to the right of the POWER button), while sending the following string to the counter:

"CLST" <cr lf>

k. Keep calibration switch depressed until display shows "donE" indicating successful non-vol memory store

l. A <space><cr lf>GPIB output is given and the calibration switch can now be released

6.7 VERIFICATION PROCEDURE

a. Connect the DC source to Inputs A and B of the UUT. Adjust the DC voltage to 4.50V using the voltmeter

b. Set up the counter for time interval A to B, Channels A and B DC coupled

c. Press the RESET key on the front panel, then the AUTO-TRIG keys for both Inputs A and B

d. Verify that the trigger LEVEL A and B displays show trigger levels between 4.45 and 4.55 volts

e. Adjust the DC source to -4.50V using the voltmeter

f. Verify that the trigger LEVEL A and B displays show trigger levels between -4.45 and -4.55 volts

6.8 INTERNAL REFERENCE ADJUSTMENT

6.8.1 Required Equipment

a. 1 MHz frequency standard. Use Racal-Dana Model 9475 or its equivalent

b. Oscilloscope. 350 MHz, B/W, 4-channel

6.8.2 There are two internal reference oscillators available for the 1995/1996.

6.8.3 The calibration procedure for the standard oscillator is a single variable capacitor adjustment, accessible at OSC ADJ on the rear panel. The Option 04E has two adjustments (COARSE and FINE), accessible at the rear panel.

6.8.4 **Reference Oscillator Frequency Check**

a. Select the following control settings:
(home state at power-up)

FUNCTION	FREQ A
GATE TIME	1second
INPUT A	
SLOPE	⨍
COUPLING	DC.
TRIGGER LEVEL	AUTO

b. Connect the 1 MHz frequency standard to Input A

c. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following equation:

Internal oscillator frequency = (2E6–display) x 10

d. Some examples of various counter readings and the frequency difference that is indicated are shown below:

Counter Display	Internal Reference Oscillator
999.9950 E3	10,000.05000 kHz
1.0000000 E6	10,000.00000 kHz
1.0000025 E6	9,999.97500 kHz

6.8.5 **Adjustment Procedure**

a. Connect the 1 MHz frequency standard to the vertical input of the oscilloscope and connect the OUT REF signal from the rear panel of the counter to the external trigger of the oscilloscope (see wiring diagram below)

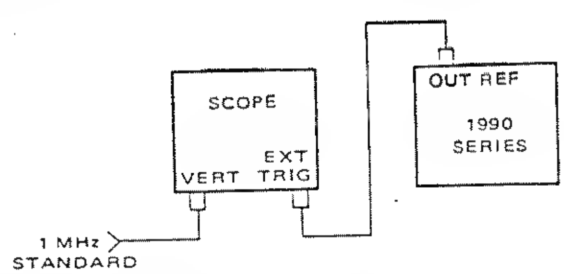


Figure 6.1 – Internal Reference Adjustment Procedure

b. Set oscilloscope controls as follows:

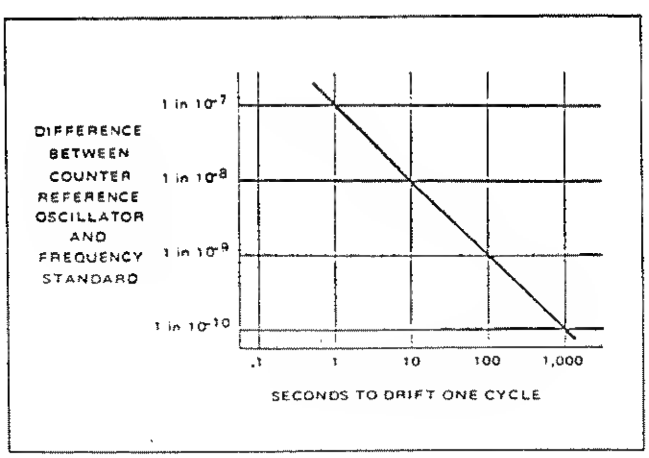
TRIGGER	
SLOPE:	⎍
COUPLING:	AC
SOURCE:	EXT
SWEEP MODE	
NORM TRIGGER	
SWEEP:	.05 μs
CHANNEL	
INPUT:	AC
volts/div	Depends on amplitude of frequency standard
TRIGGER LEVEL:	Center of mechanical span

c. Adjust the trigger level for an oscilloscope display of the frequency standard output

d. If the counter is equipped with the standard reference oscillator, adjust OSC ADJ on the rear panel for an oscilloscope display that is as stationary as possible (i.e., does not drift to the left or right)

e. If the instrument is equipped with an optional high-stability reference oscillator, use the COARSE and FINE adjustment controls to perform step d

f. To determine the drift rate of the calibrated instrument, measure the time it takes the oscilloscope pattern to drift 5 divisions on the oscilloscope. The oscillator drift can be determined from the figure shown below



6.3 PERFORMANCE TEST PROCEDURES

6.3.1 Power-on/self-test and home state conditions are described in Subsections 3.2.2 and 3.2.3, respectively. Refer to this information as necessary.

6.3.2 Set up the 1995/1996 and test equipment as shown in the following figures provided for each test procedure. Set the control and inputs as noted in each table and monitor the counter's readout for the indicated values.

Table 5.2 -Self Test

Applied Frequency	Min. Input Signal Level	Tolerance	Counter Resolution	Special Notes
Internal 5 MHz	Internal		10 ms gate (default)	

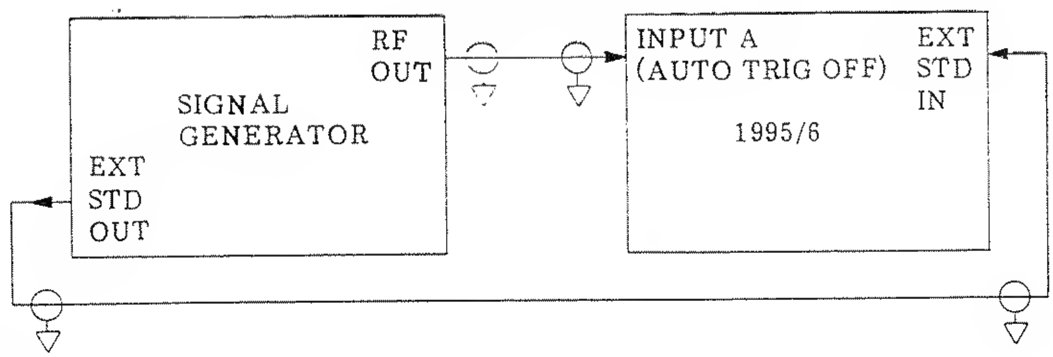
PROCEDURE

1. Power up the 1995/6.
2. Press the "CHECK" button for 3 seconds until all LEDs light.
3. After the release of "CHECK" button, the unit will be in self-test and the word "test" will appear on the display
4. This test takes a maximum of 75 seconds and any existing error conditions will be displayed momentarily.
5. When the self-test is completed, the unit returns to "CHECK" mode with 5 MHz on the display.

Table 6.3 – Input A Sensitivity Performance Test, I

Applied Frequency : Performance Standard	Input Signal Level	Tolerance	Counter Resolution	Special Notes
200 MHz 100 MHz	50.0 mV rms 25.0 mV rms	± .2 Hz ± .1 Hz	1-sec gate 1-sec gate	Use an AC voltmeter to verify applied input signal level into 50-Ω load before applying to UUT

Test Setup



PROCEDURE

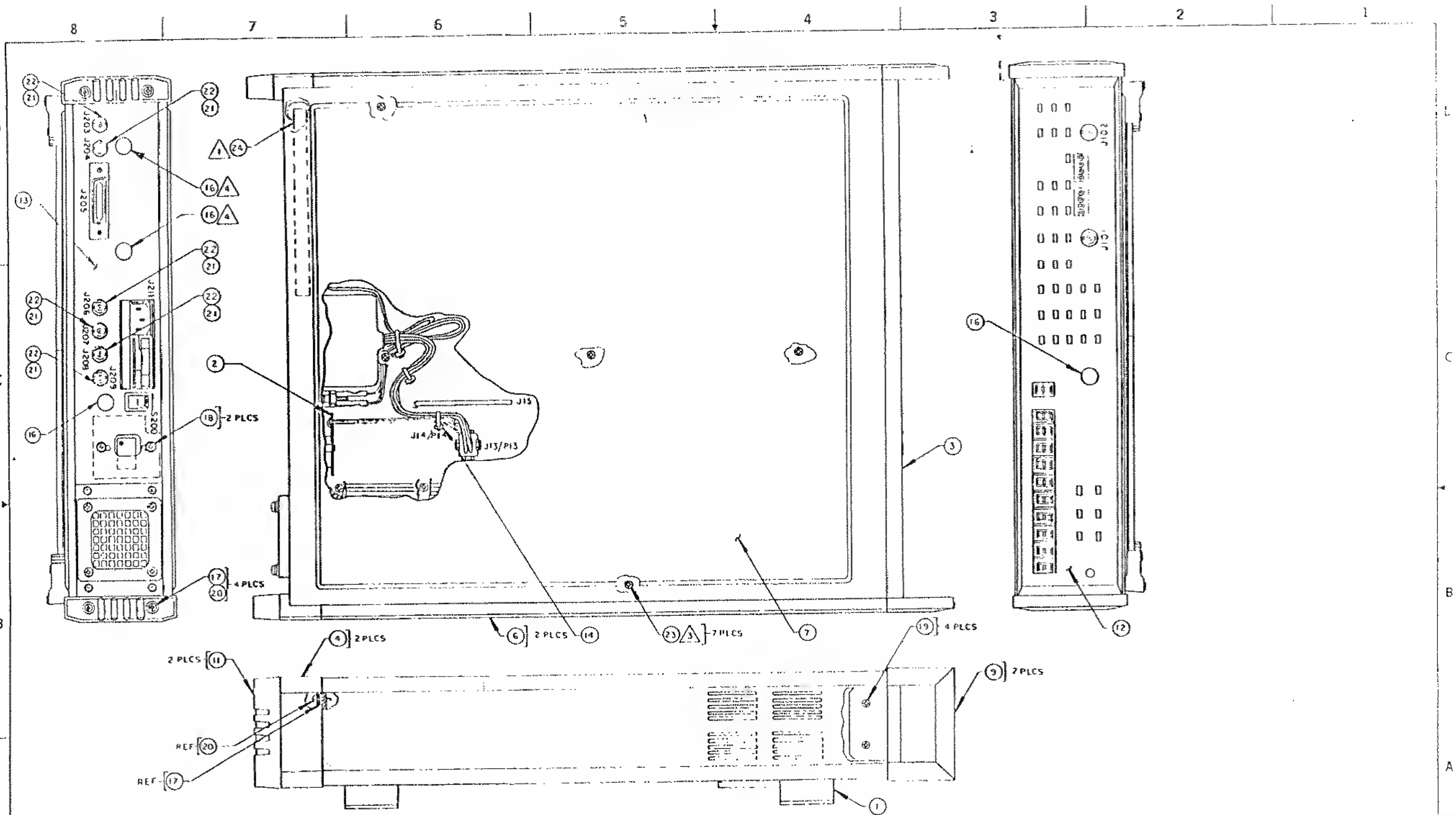
1. Power up the 1995/6.

2. Set the 1995/6 as follows: FREQ A
Input A 50 ohms input impedance
Gate time 1 sec
Disable input A auto trigger
Set input A trigger level to 0.00V

3. Connect the 1995/6 and signal generator as shown above.

4. Apply the inputs shown in the table above and verify that the measurements taken are within the specified tolerances.

SECTION 7 DRAWINGS



4. PLASTIC HOLE PLUGS ITEM #16 SHOULD BE MOVED TO RELATING HOLES IN FRONT PANEL WHEN CHANNEL A & B REAR INPUT IS INSTALLED.

3. INSTALL SCREWS (ITEM #23) IN MOTHERBOARD PRIOR TO INSTALLING COVERS.

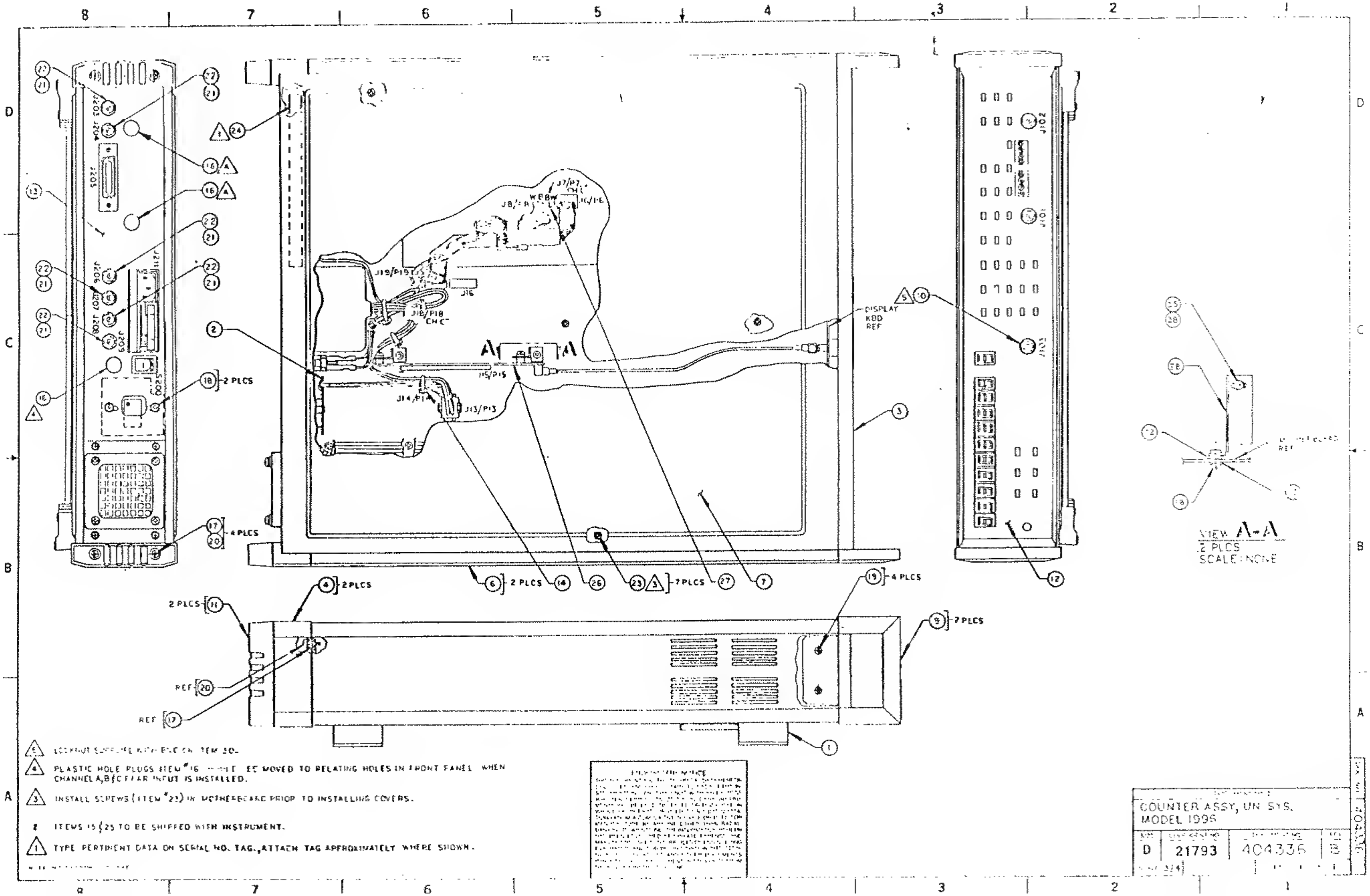
2. ITEMS 15 & 25 TO BE SHIPPED WITH INSTRUMENT.

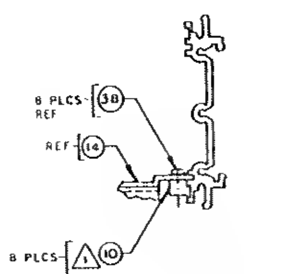
1. TYPE PERTINENT DATA ON SERIAL NO. TAG., ATTACH TAG APPROXIMATELY WHERE SHOWN.

PROPRIETARY NOTICE

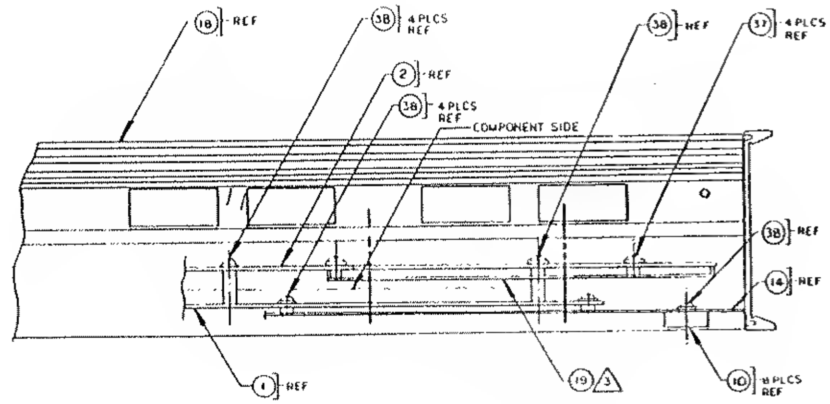
COUNTER ASSY, UN SYS. MODEL 1995			
D	21793	404335	B

DOC NO 404335


COUNTER ASSY, UN SYS.
MODEL 1996
D
21793
404336
VIEW A-A
2 PLCS
SCALE: NONE
INSTALL SCREWS (ITEM #23) IN MOTHERBOARD PRIOR TO INSTALLING COVERS.
ITEMS 15 & 25 TO BE SHIPPED WITH INSTRUMENT.
TYPE PERTINENT DATA ON SERIAL NO. TAG., ATTACH TAG APPROXIMATELY WHERE SHOWN.
DISPLAY
KBD
REF
J203
J204
J205
J206
J207
J208
J209
J211
S200
J101
J102
J103
J16
2 PLCS
4 PLCS
7 PLCS



SECTION A-A
SCALE: NONE



SECTION B-B
SCALE: NONE

3 SHIELD, ITEM NO. 19 MUST BE ATTACHED TO PCB ASSY ITEN NO. 2 PRIOR TO INSTALLING IN CHASSIS.

2 RETAINING NUTS SUPPLIED WITH BNC'S ON ITEM NO. 2.

1 INSTALL & ORIENT ITEM NO. 10 AS SHOWN.

NOTES

PROPRIETARY NOTICE

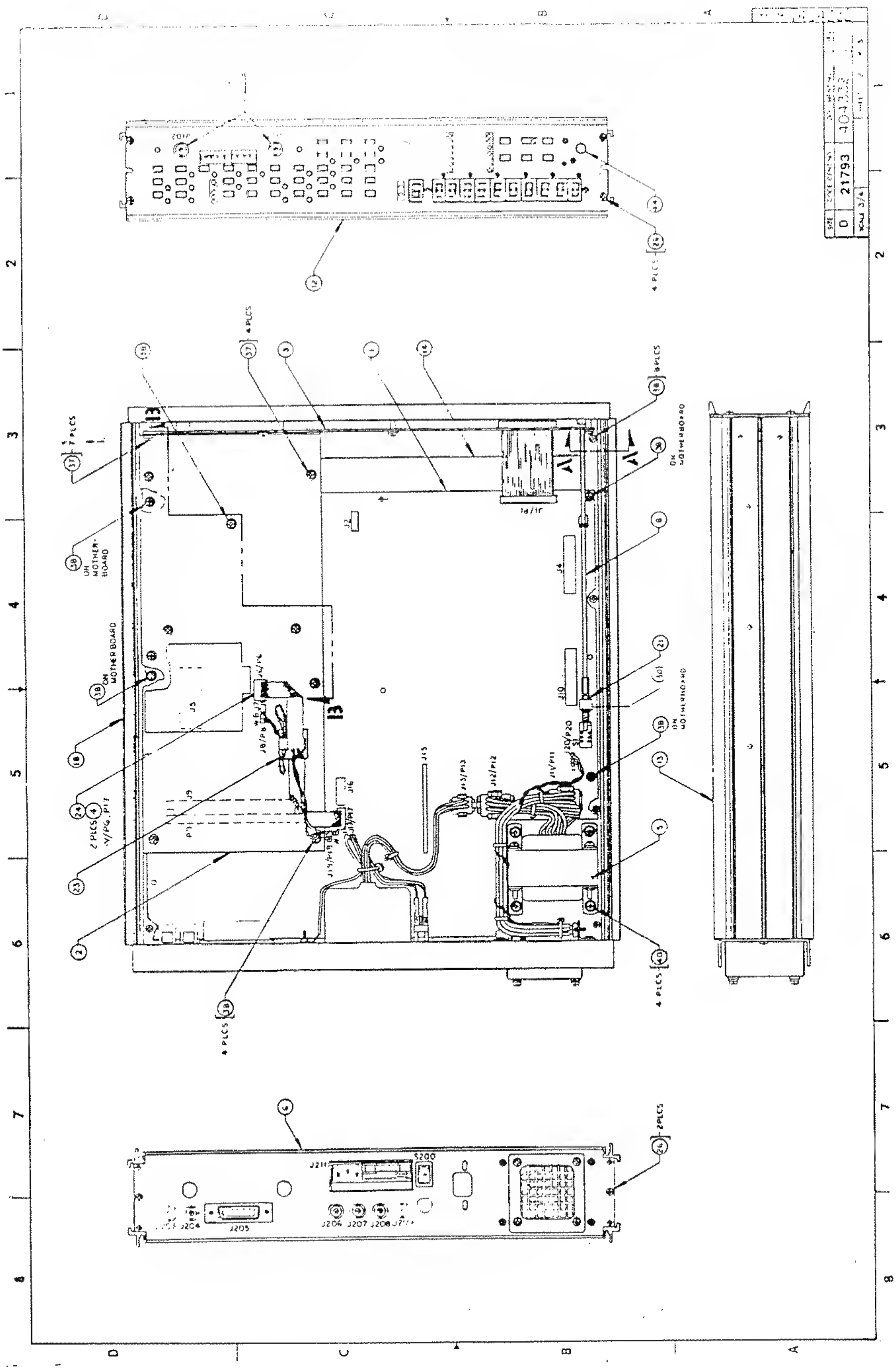
RACAL-DANA Instruments Inc.

DOCUMENT TITLE

CHASSIS ASSY

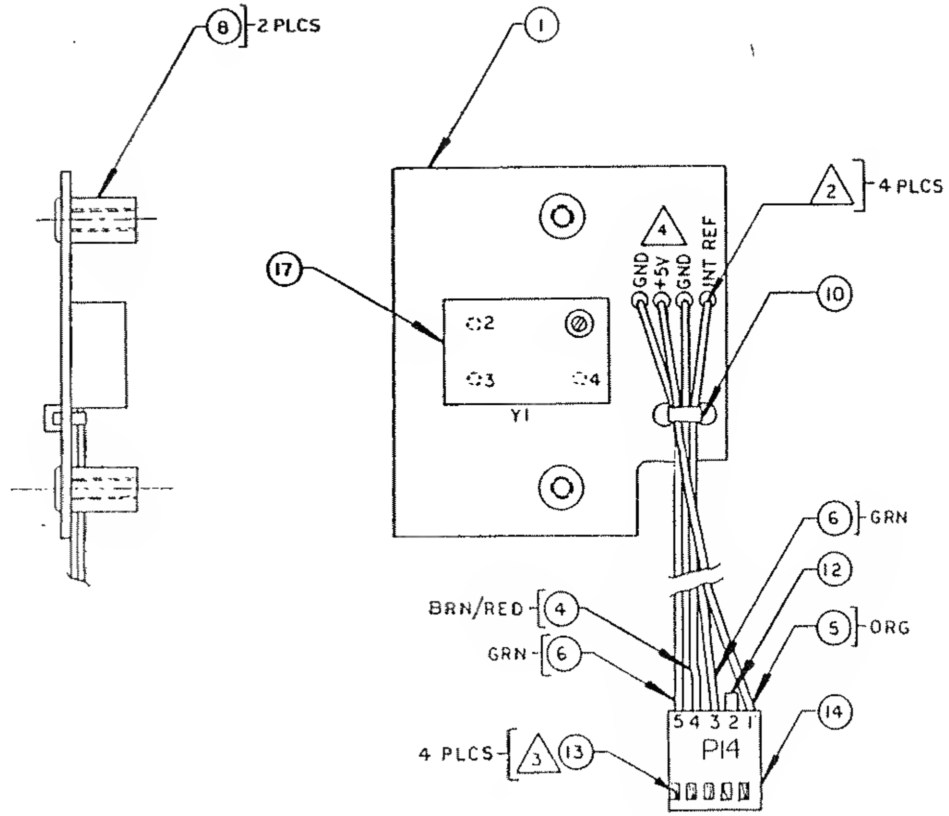
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404332	

SCALE 3/4



D
21793
4 PLCS
2 PLCS
7 PLCS
8 PLCS
ON MOTHER BOARD
J204
J205
J206
J207
J208
J211
S200

NOTES UNLESS OTHERWISE SPECIFIED



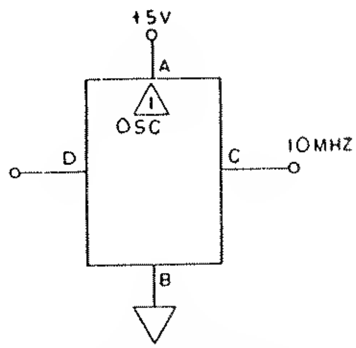
4\ NOMENCLATURE SHOWN IS ON FARSIDE OF PC BOARD.

3\ STRIP WIRE .14.

2\ STRIP WIRE .25.

1. SCHEMATIC REF NO. 431730

PCB ASSY, 10MHZ OSC.			
C	21793	401730	A



OSC. VENDOR CHART

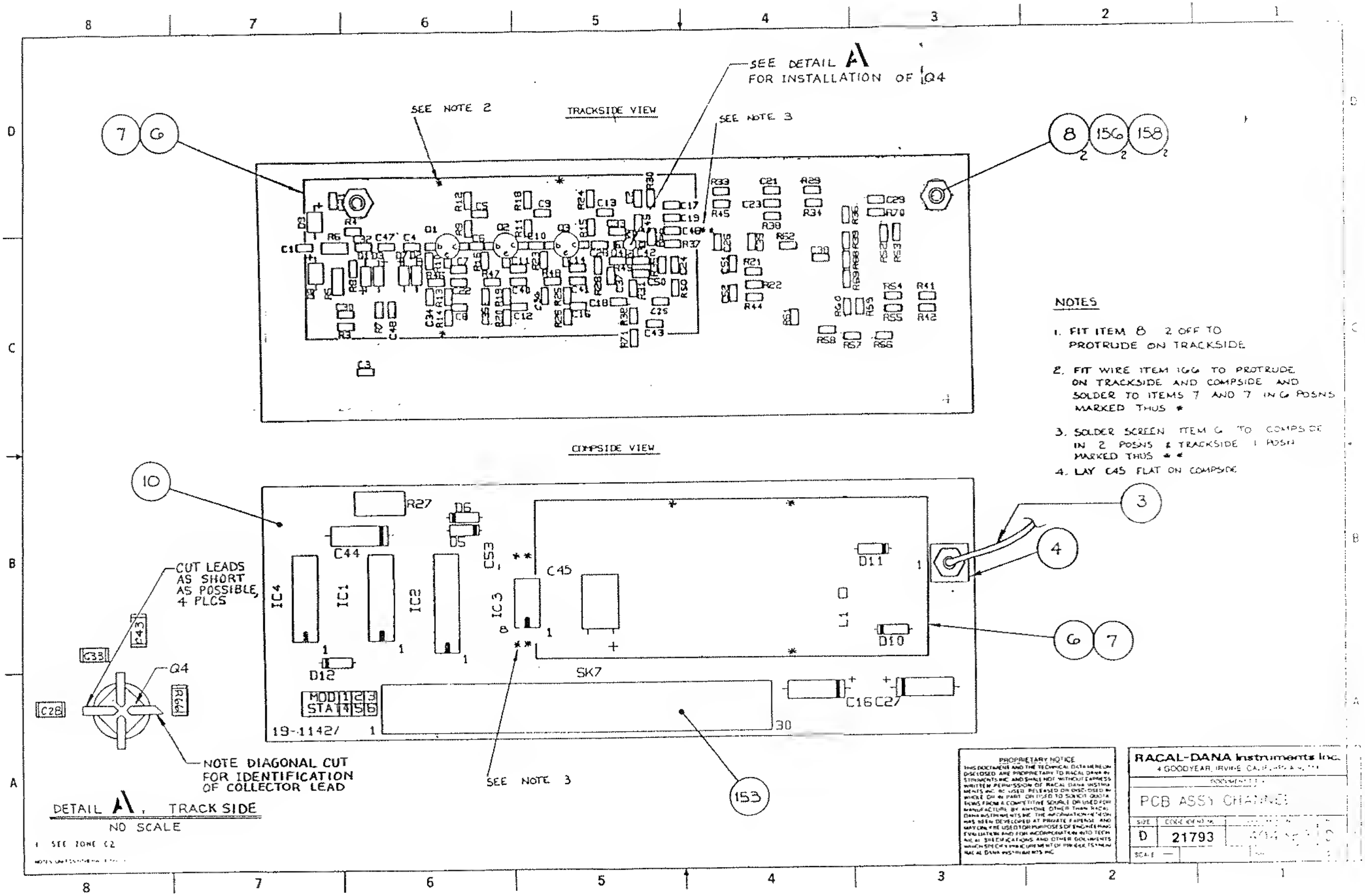
	P/N 921013 NDK	P/N 921014 TCXO	P/N 921013 SEI
A	4	2	2
B	2	4	1
C	3	1	3
D	1 (NC)	3 (NC)	4 (NC)

1. FOR SPECIFIC PIN NUMBERS REFER TO OSC. VENDOR CHART.

NOTES: UNLESS OTHERWISE SPECIFIED

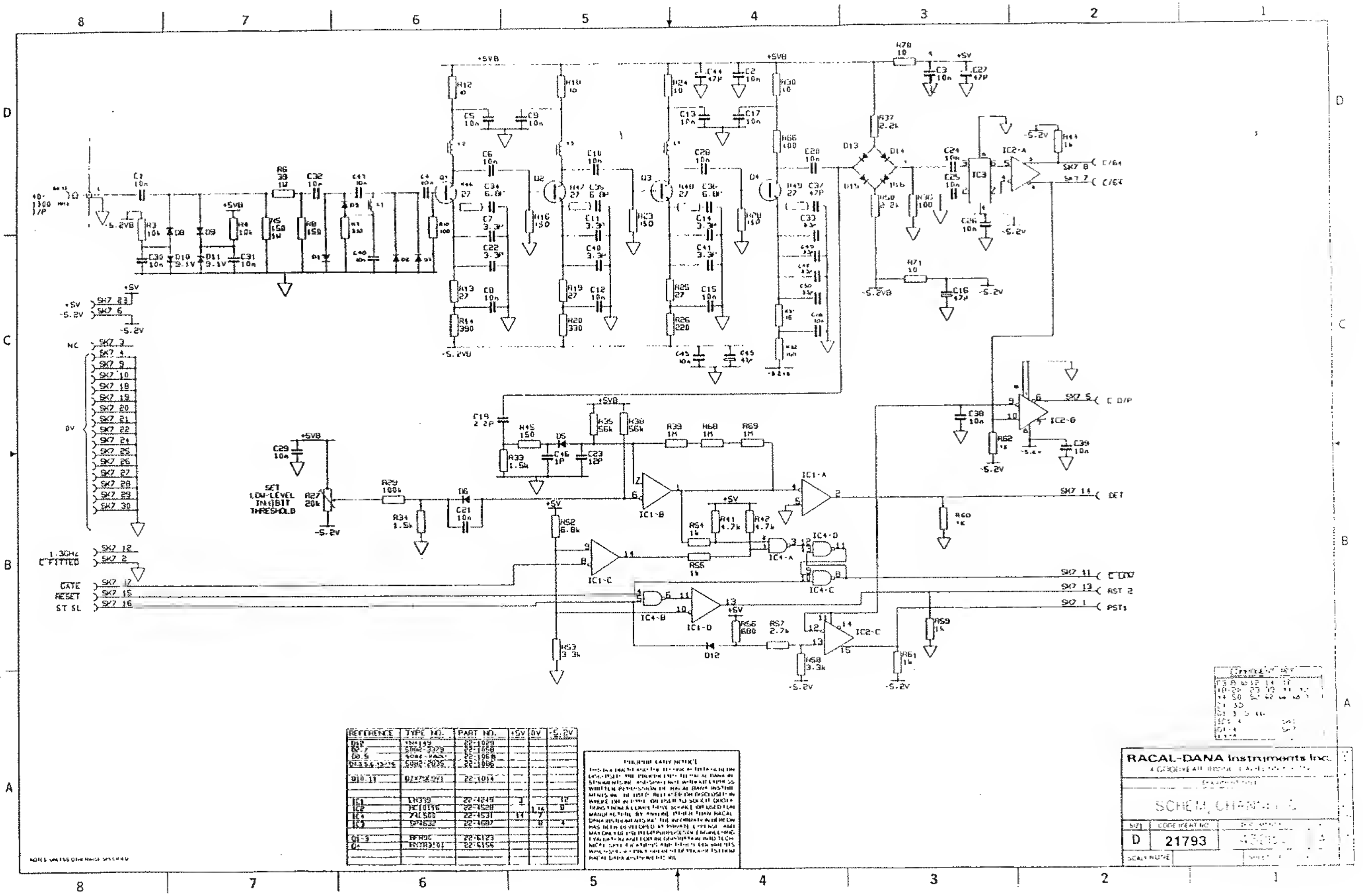
PROPRIETARY NOTICE

SCHEMATIC, 10MHZ OSC			
SIZE B	CODE IDENT NO 21793	DWG NO 431730	REV A
SCALE —			SHEET 1 OF 1

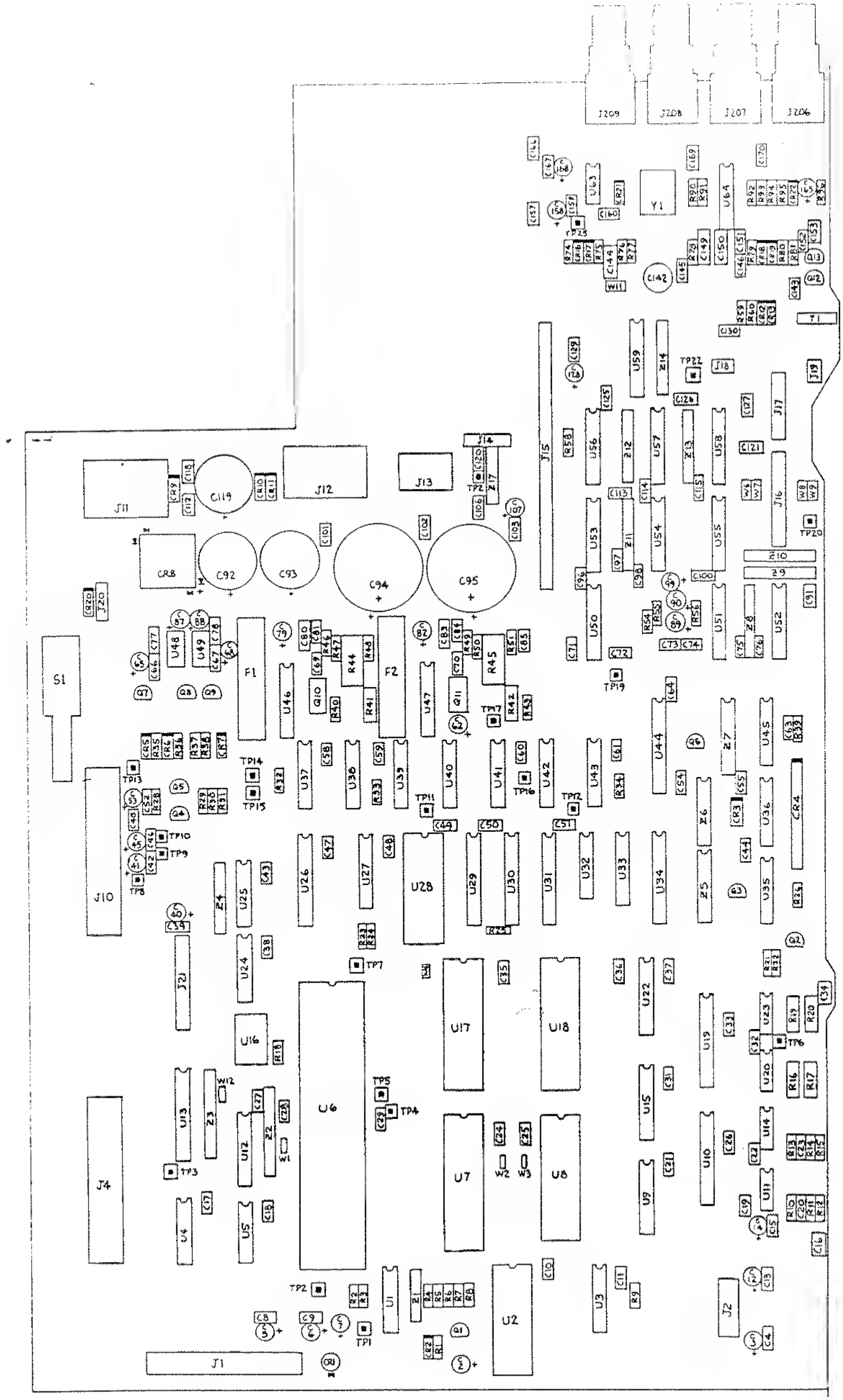


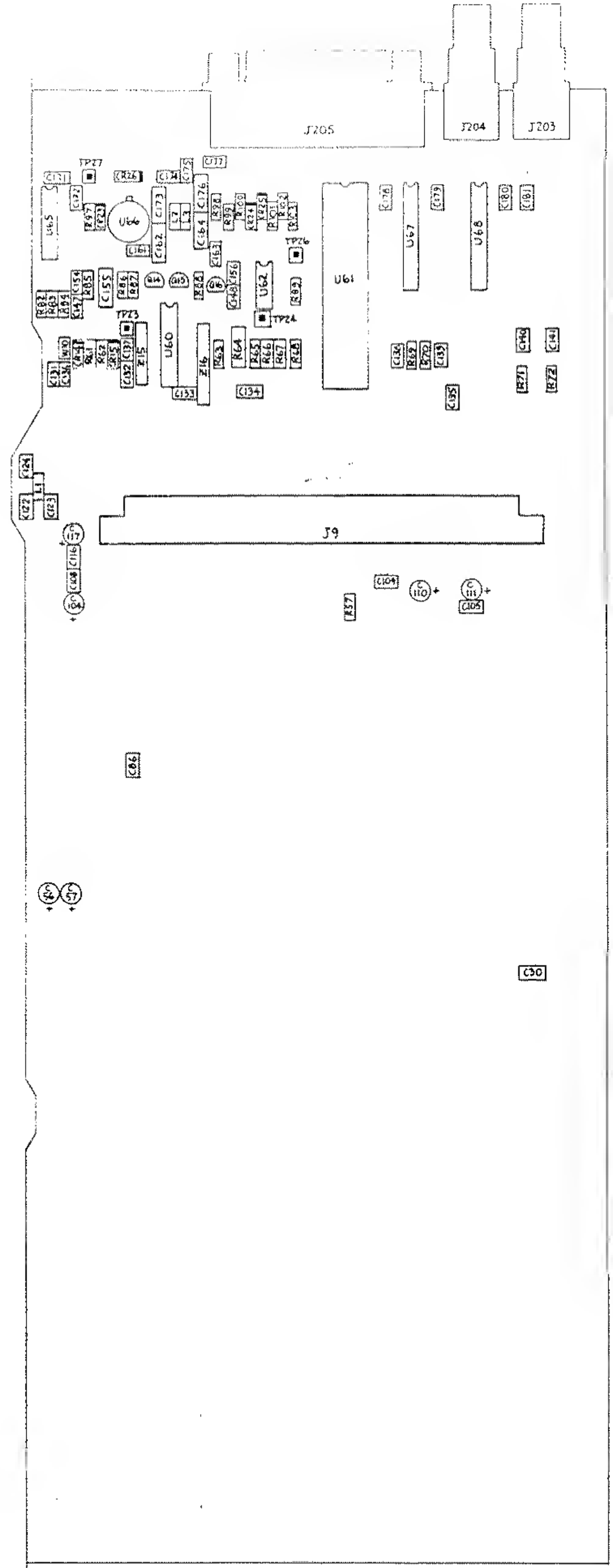
SEE DETAIL A FOR INSTALLATION OF Q4
SEE NOTE 2
TRACKSIDE VIEW
SEE NOTE 3
COMPSIDE VIEW
SEE NOTE 3
NOTES
1. FIT ITEM 8 2 OFF TO PROTRUDE ON TRACKSIDE
2. FIT WIRE ITEM 166 TO PROTRUDE ON TRACKSIDE AND COMPSIDE AND SOLDER TO ITEMS 7 AND 7 IN 6 POSNS MARKED THUS *
3. SOLDER SCREEN ITEM 6 TO COMPSIDE IN 2 POSNS & TRACKSIDE 1 POSN MARKED THUS **
4. LAY C45 FLAT ON COMPSIDE
CUT LEADS AS SHORT AS POSSIBLE, 4 PLCS
NOTE DIAGONAL CUT FOR IDENTIFICATION OF COLLECTOR LEAD
DETAIL A, TRACK SIDE
NO SCALE
19-1142/
MOD 1 2 3
STA 4 5 6
SK7
PROPRIETARY NOTICE
RACAL-DANA Instruments Inc.
4 GOODYEAR, IRVINE
PCB ASSY CHANNEL
D
21793

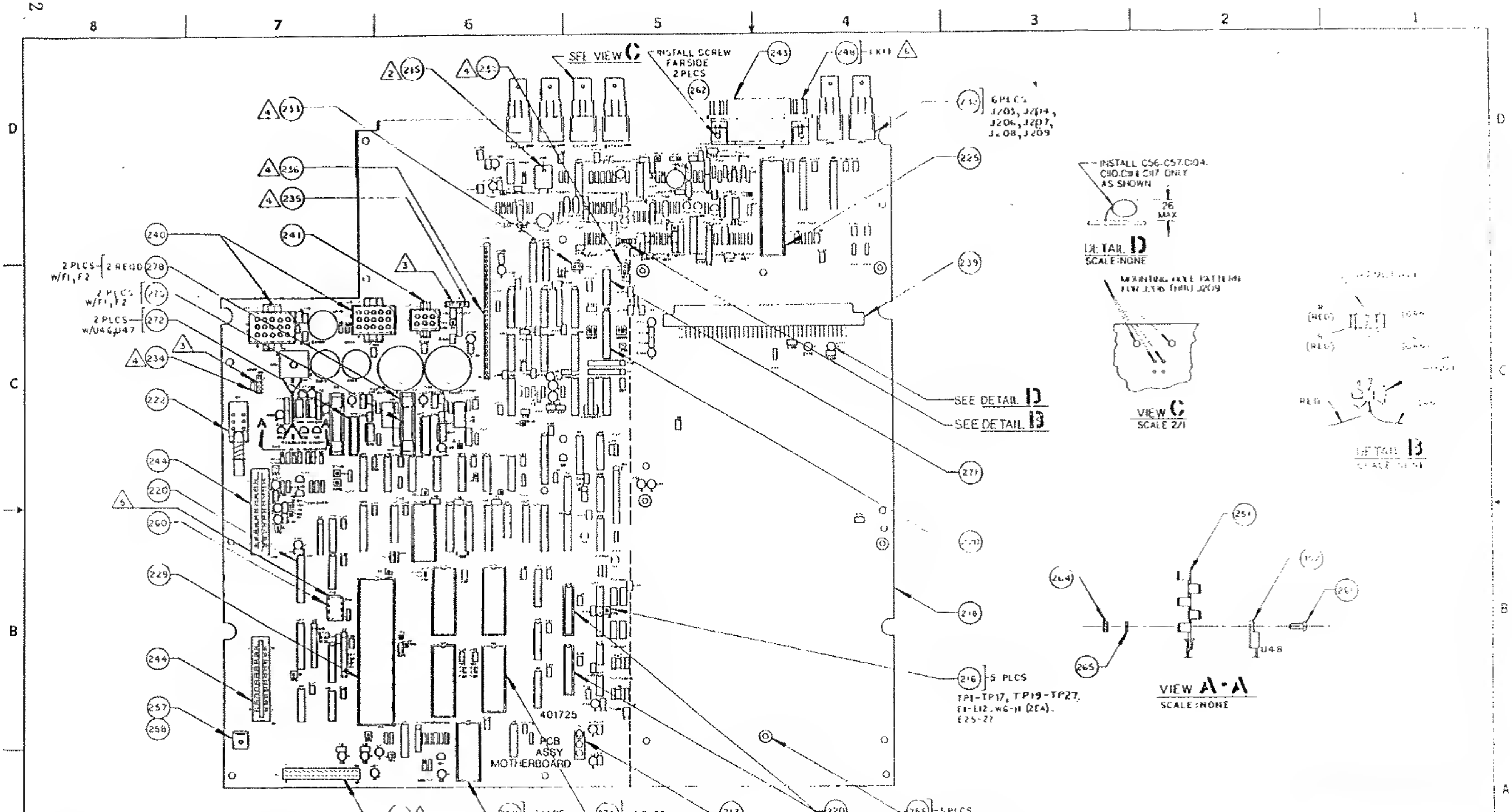
7-9



REFERENCE	TYPE NO.	PART NO.	+5V	0V	-5.2V
D12	1N4149	22-1029			
D2,7	5082-3379	22-1050			
D8,9	[illegible]	22-1068			
D1,3,5,6,13-15	5082-2835	22-1006			
D10,11	BZX79C9V1	22-1014			
IC1	LM339	22-4249	3		12
IC2	MC10116	22-4528		1,16	8
IC4	74LS00	22-4531	14	7	
IC3	SP4632	22-4687		8	4
Q1-3	BFR90	22-6123			
Q4	[illegible]	22-6155			




J205
J204
J203
J9
U61
U60
U62
U66
U67
U68
U65

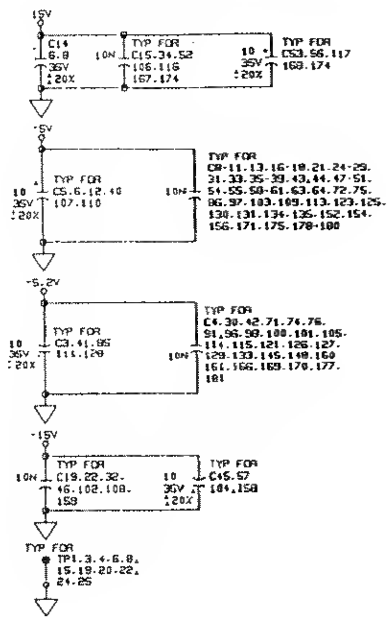


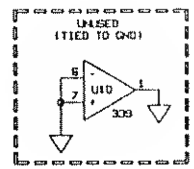
6. DISCARD NUTS (2) & LOCKWASHERS (2) SUPPLIED WITH ITEM 248
5. SHARP CORNER INDICATES PIN 1 ON ITEM 282.
4. INSTALL WITH SHORT LEADS IN PCB.
3. AFTER INSTALLATION CUT PIN INDICATED FLUSH WITH HOUSING.
2. SOLDER ITEM 215 TO CASE OF Y1 AS SHOWN.
1. REFERENCE SCHEMATIC 431725.

PROPRIETARY NOTICE

RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA

DOCUMENT TITLE	PCB ASSY, MOTHERBOARD		
SIZE	CODE IDENT NO.	DOCUMENT NO.	REV
D	21793	401725	K





REF. DES.	IC TYPE	+5V PIN NO.	+15V PIN NO.	GND PIN NO.	AGND PIN NO.	DGND PIN NO.	-5.2V PIN NO.	[illegible] PIN NO.
U68	75161	20		10				
U67	75160	20		10				
U66	710			1			4	
U65	74LS132	14		7				
U63	TL081		7					
U62	686	1		5.6			4	
U61	9914A	40		20				
U57.58.60	10102			1.16			8	
U55.59	10231			1.16			8	
U54	10130			1.16			8	
U52	10216			1.16			8	
U51.53	10125	9		16			8	
U50.56	10124	9		16			8	
U49	7915			1				
U48	7815			2				
U42	74LS08	14		7				
U41	74LS54	14		7				
U40	74LS51	14		7				
U39	74LS04	14		7				
U38.43	74LS74	14		7				
U37	74LS32	14		7				
U33	74LS153	16		8				
U32	74LS06	14		7				
U29.31.34.44	74LS273	20		10				
U28	8254	24		12				
U27	74LS367	16		8				
U26	80048	20		10				
U25	74HC32	14		7				
U24	74F32	14		7				
U20	1404		2	4				
U17.18	27512	28		14				
U16	OSCILLATOR	14		7				
U14.23	OP07		7					
U13.30	74LS244	20		10				
U12	74LS148	16		8				
U11	LF412		8					
U10.19	7545	18			2	3		
U9.15.22	74LS138	16		8				
U7.8	TMM2016P	20		14				
U6	68000	14.49		16.53				
U5	74F04	14		7				
U4	74F00	14		7				
U3	74F20	14		7				
U2	5516A	24		12				
U1	339	3		12				

IC POWER CONNECTIONS

REF. DES.	TYPE	PINS
Z17	10K	4.5.6
Z16	500	4.5.6.7.8
Z15	470	5.6
Z14	500	2.5.7
Z11	500	6
Z10	270	8
Z9	160	8
Z8	500	7.8
Z6	6K	11
Z4	4.7K	8
Z3	10K	10
U64E	3046	12.14
U59B	10231	10.11.12.13.14.15
U58D	10102	9.12.13.15
U57D	10102	10.11.14
U50D	10124	2.4.5.6
U37D	74LS32	11.12.13
U37C	74LS32	1.2.3

UNUSED LOGIC & NETWORKS

HIGHEST	NOT USED
Z17	
Y1	
W12	
U68	U21
TP27	
T1	
S1	
R103	R73.52.53
Q16	
L3	
J209	
F2	
E27	
CR26	
C181	C1.151

REF. DESIGNATIONS

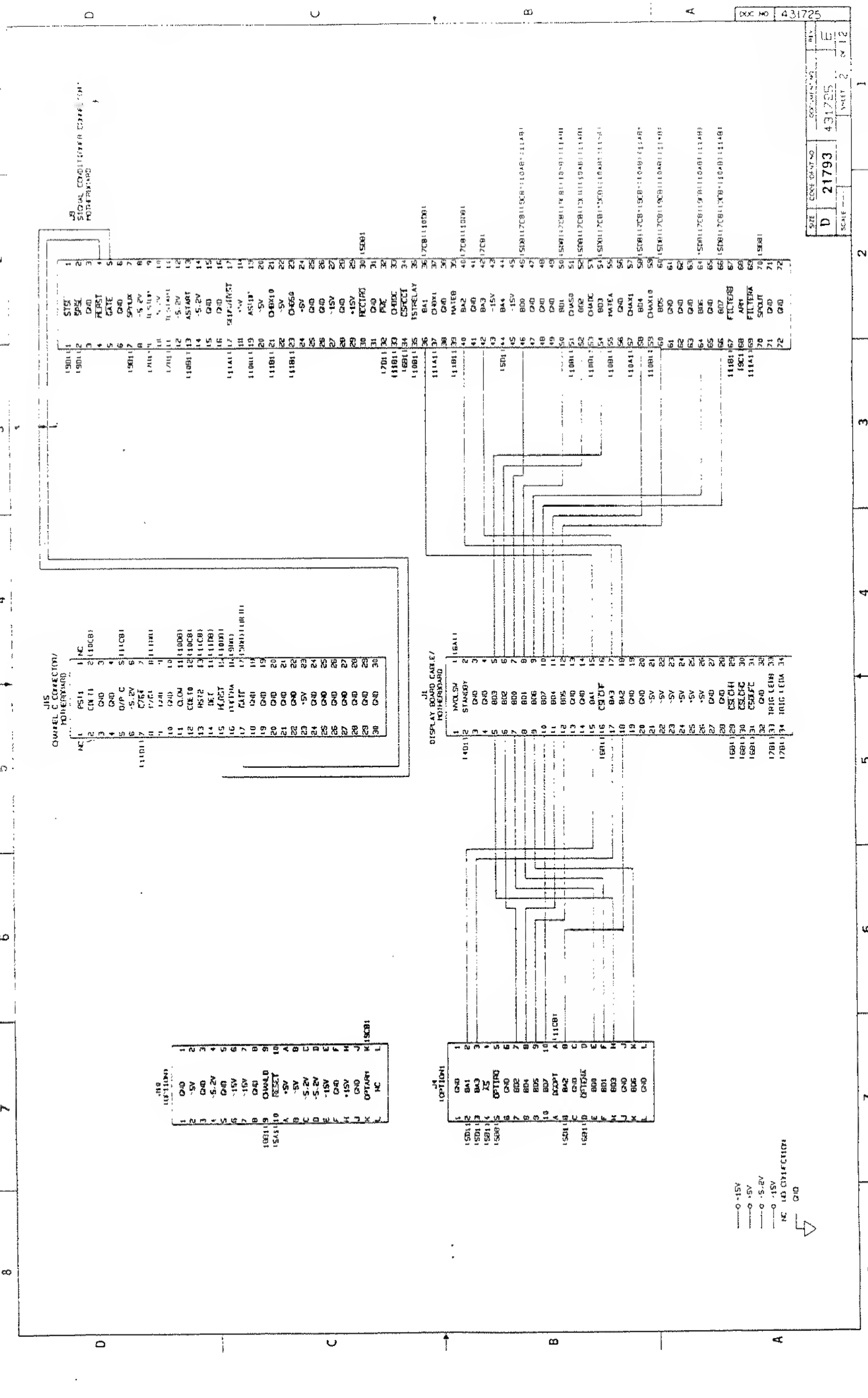
PROPRIETARY NOTICE

6. FOR LINES TERMINATED WITH (2A3), "2" INDICATES SHEET #, "A" INDICATES SHEET VERTICAL ZONE, "3" INDICATES SHEET HORIZONTAL ZONE.
5. FOR LINES TERMINATED WITH "(SHT 2)", GO TO INDICATED SHT. FOR ORIGIN.
4. CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 100V UNLESS OTHERWISE SPECIFIED.
3. RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W UNLESS OTHERWISE SPECIFIED.
2. RESISTOR NETWORKS ±2%.
1. CHOKES ARE IN MICROHENRYS.

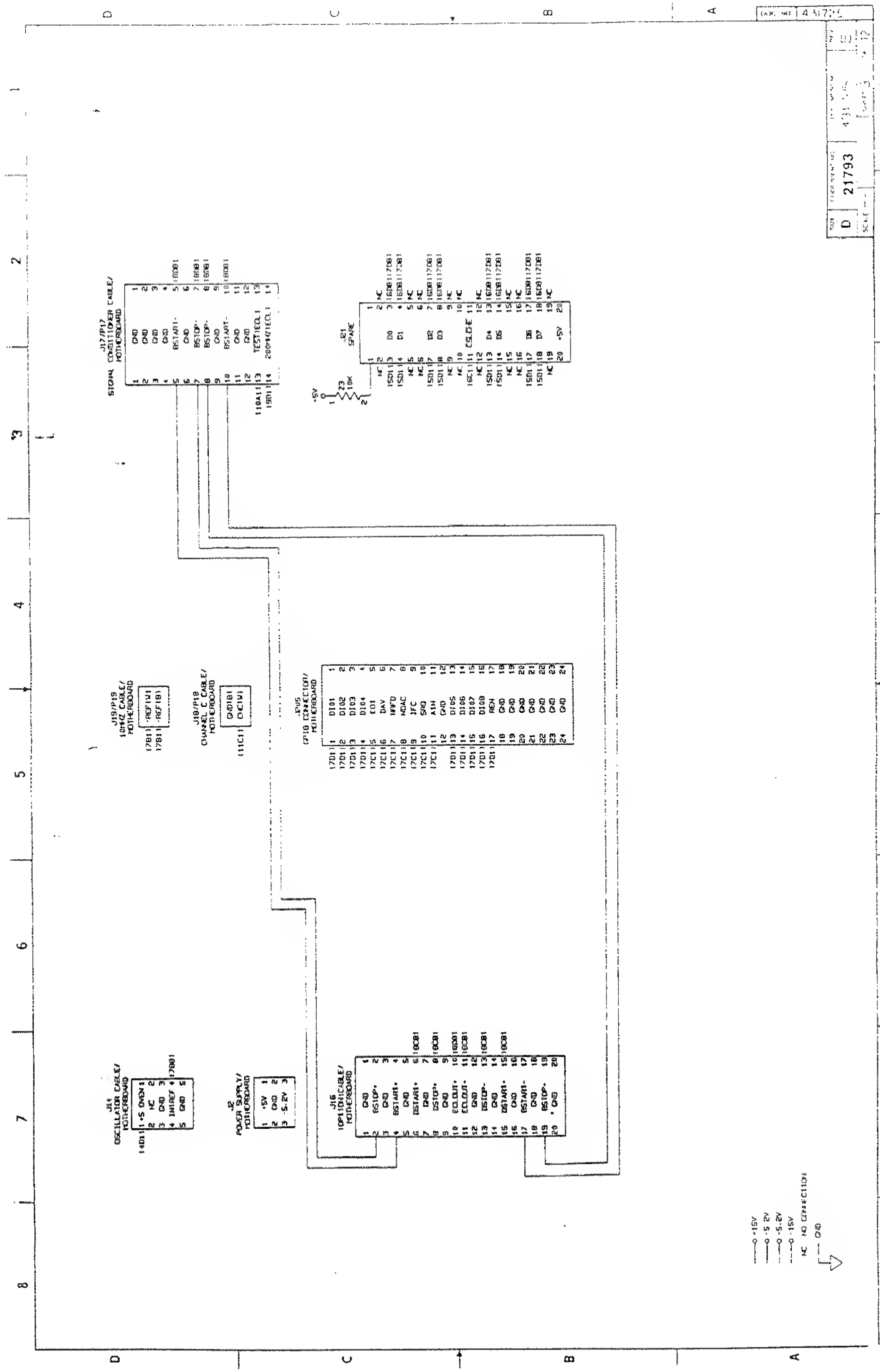
NOTES UNLESS OTHERWISE SPECIFIED

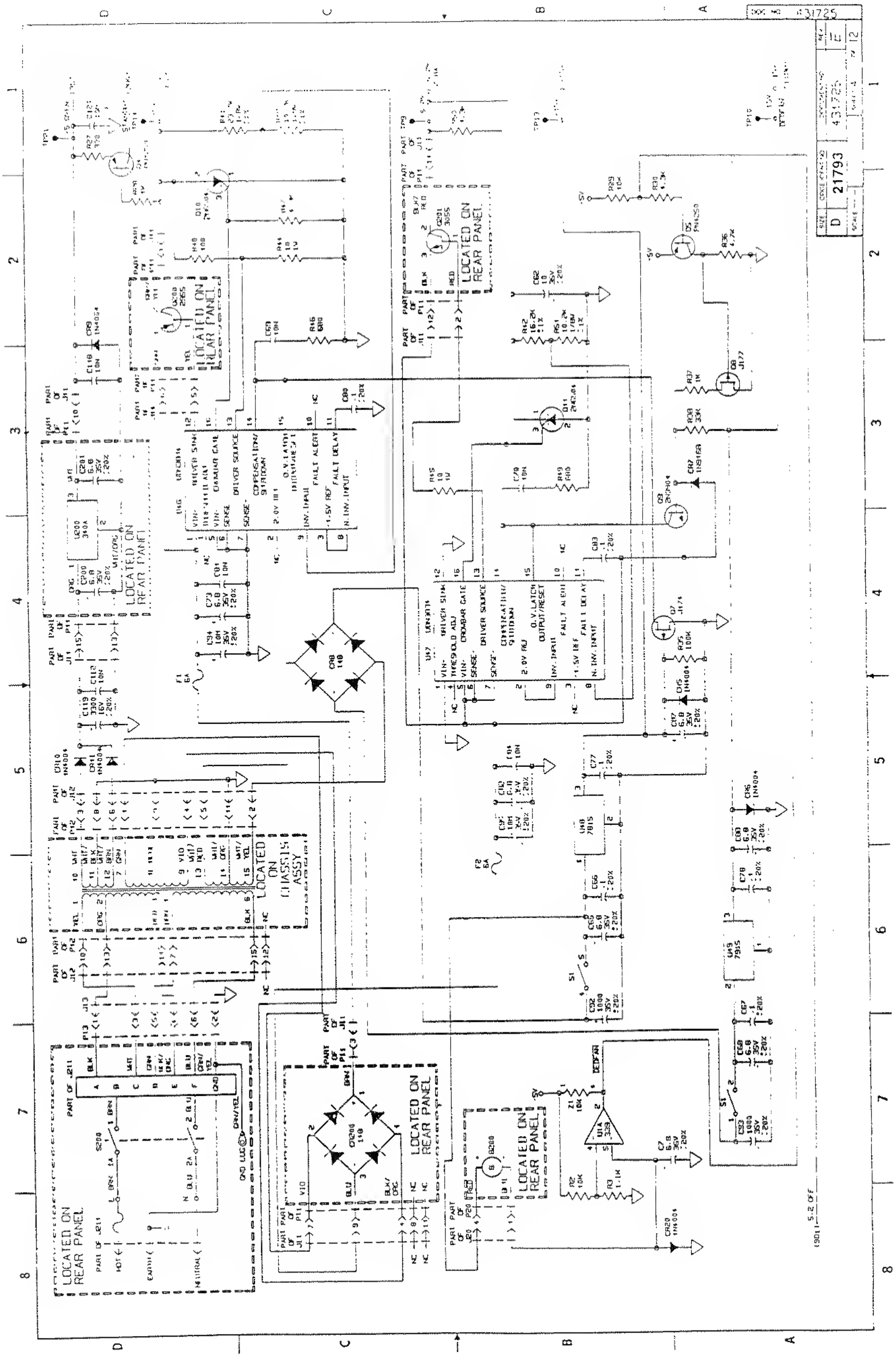
SCHEM, MOTHERBOARD

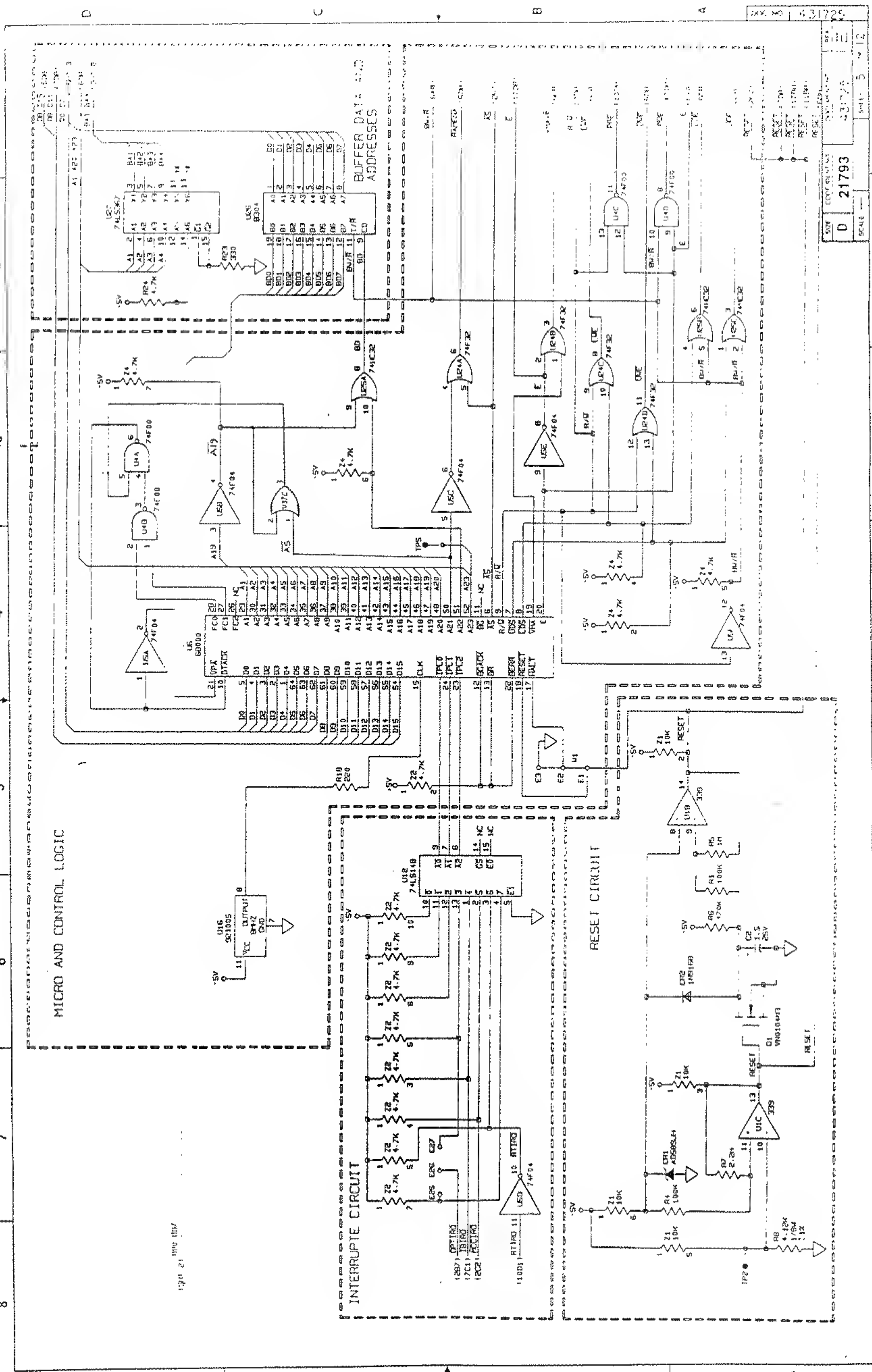
SIZE	CODE IDENT NO.	DOC. NO.
D	21793	431725

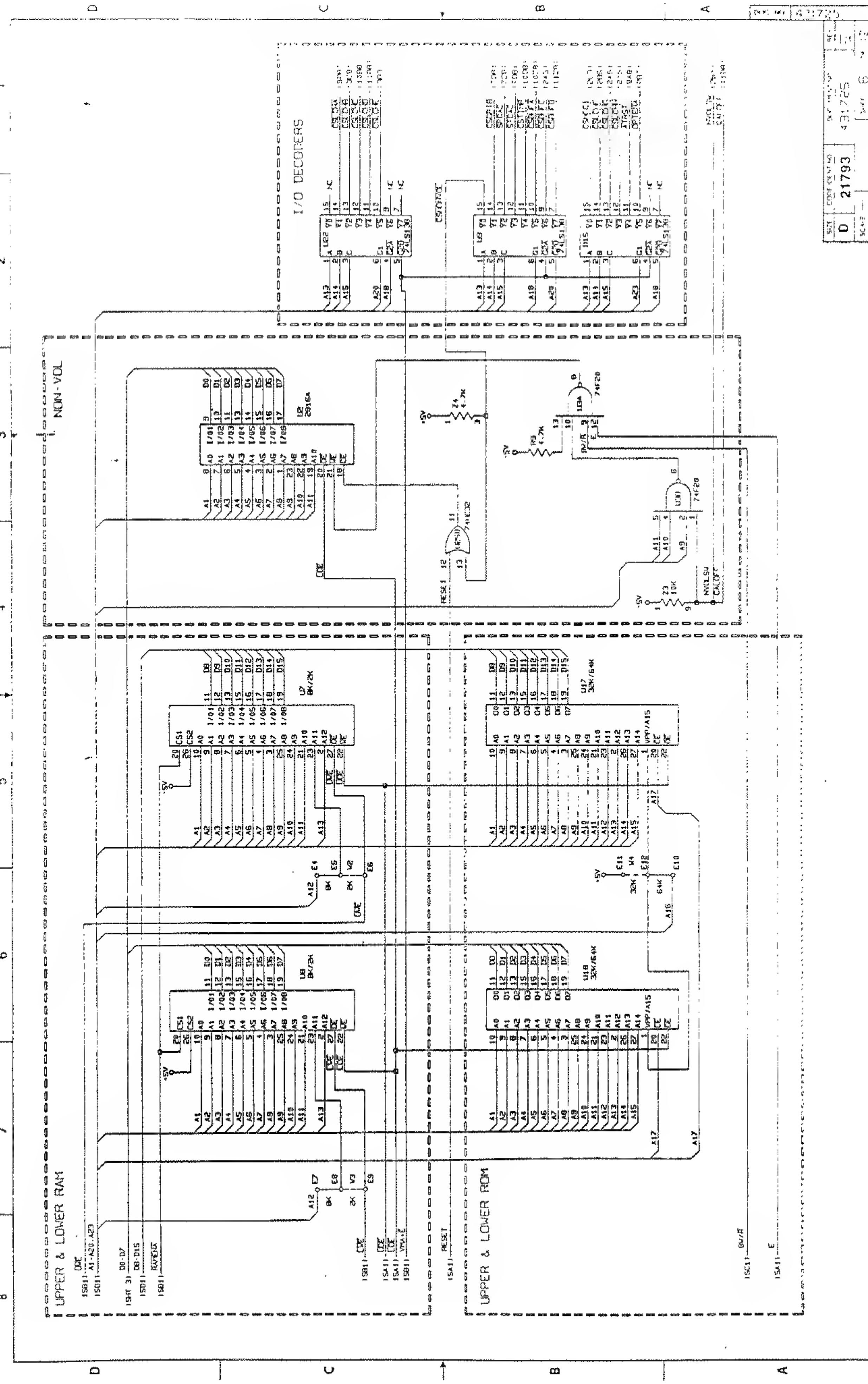


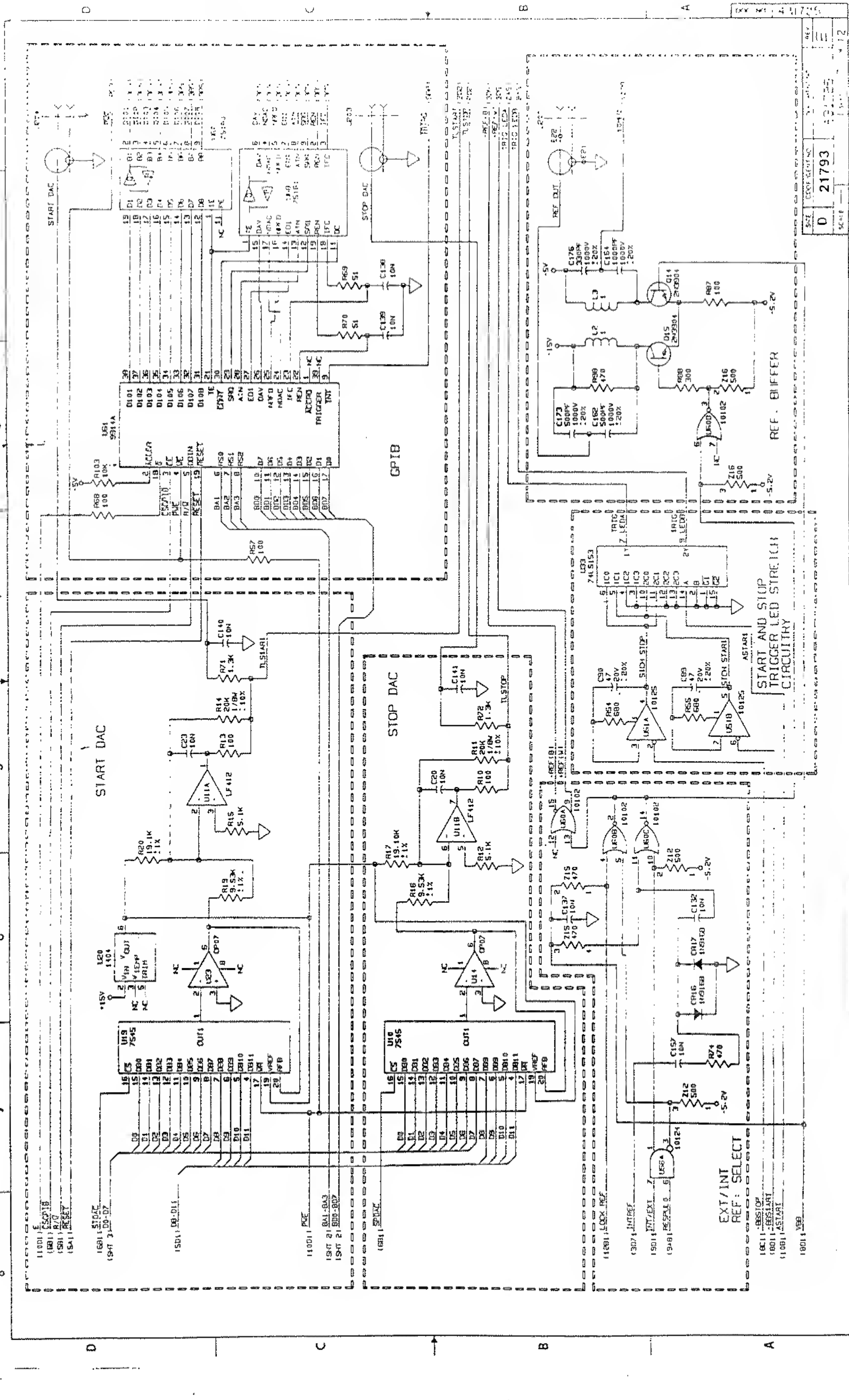
DOC NO 431725
CODE IDENT NO 21793
SIZE D
J15 CHANNEL C CONNECTOR/ MOTHERBOARD
J1 DISPLAY BOARD CABLE/ MOTHERBOARD



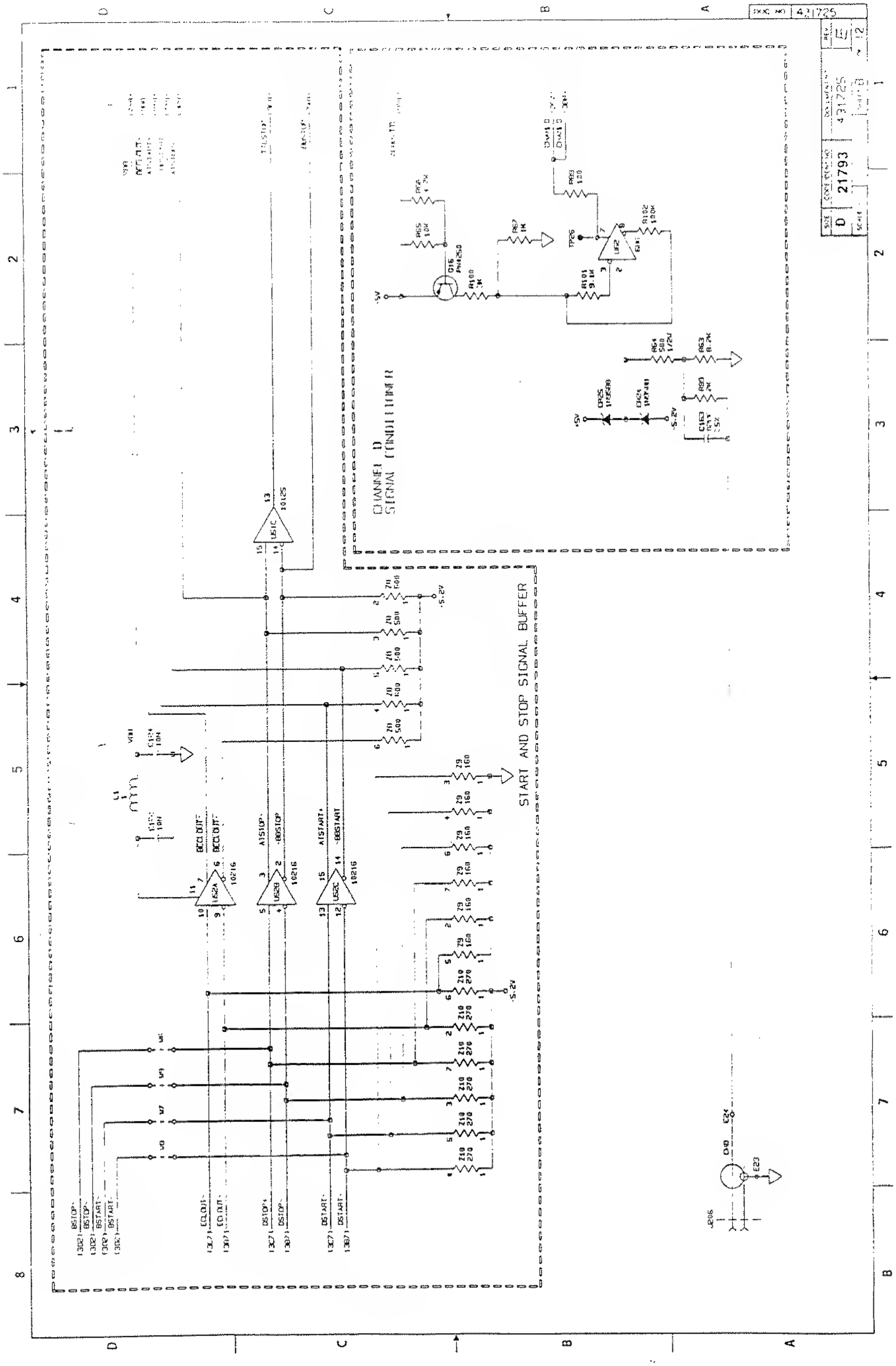

431725
21793
LOCATED ON REAR PANEL
LOCATED ON CHASSIS ASSY

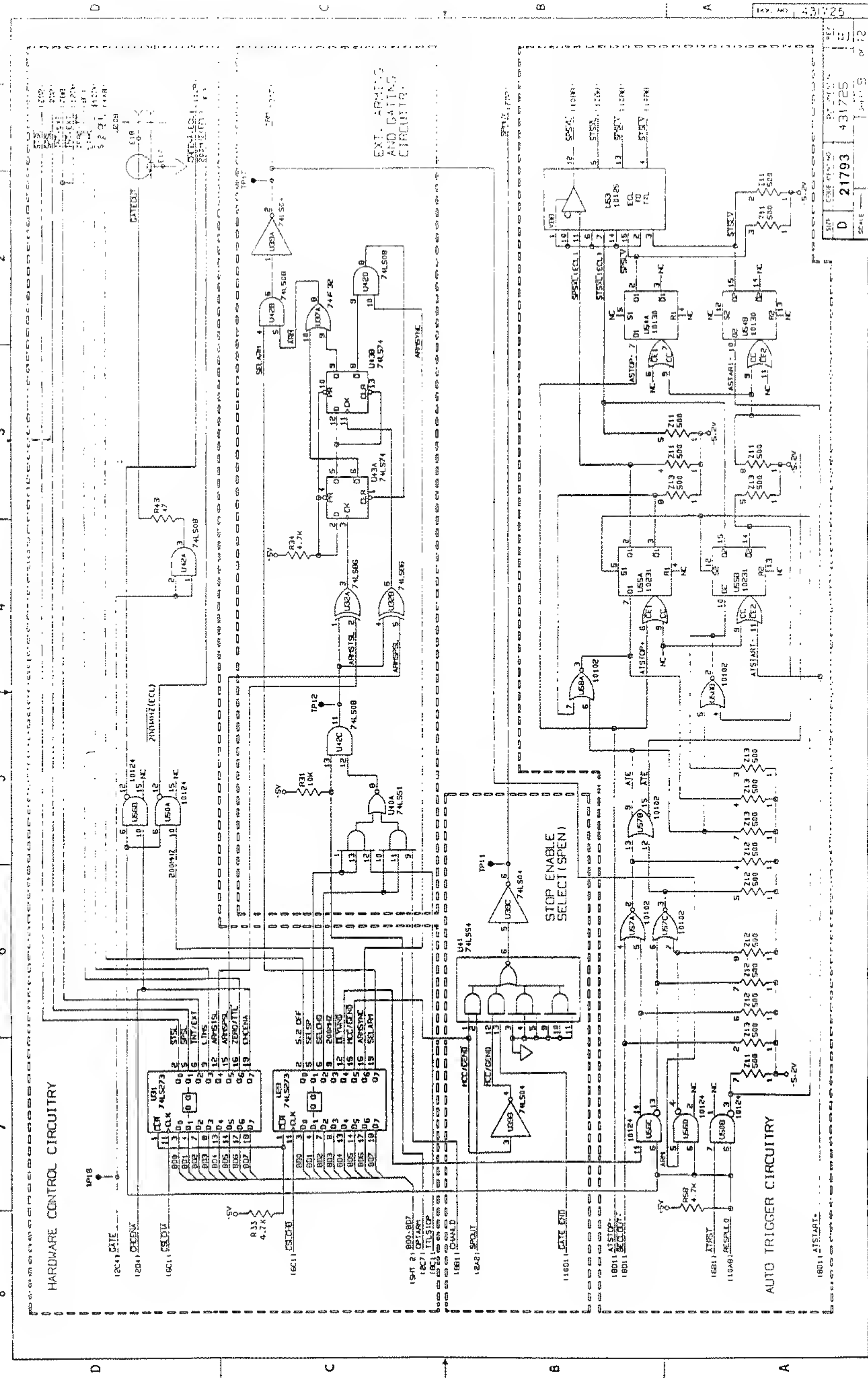

MICRO AND CONTROL LOGIC
BUFFER DATA AND ADDRESSES
INTERRUPT CIRCUIT
RESET CIRCUIT
21793


I/O DECODERS
NON-VOL
UPPER & LOWER RAM
UPPER & LOWER ROM
21793

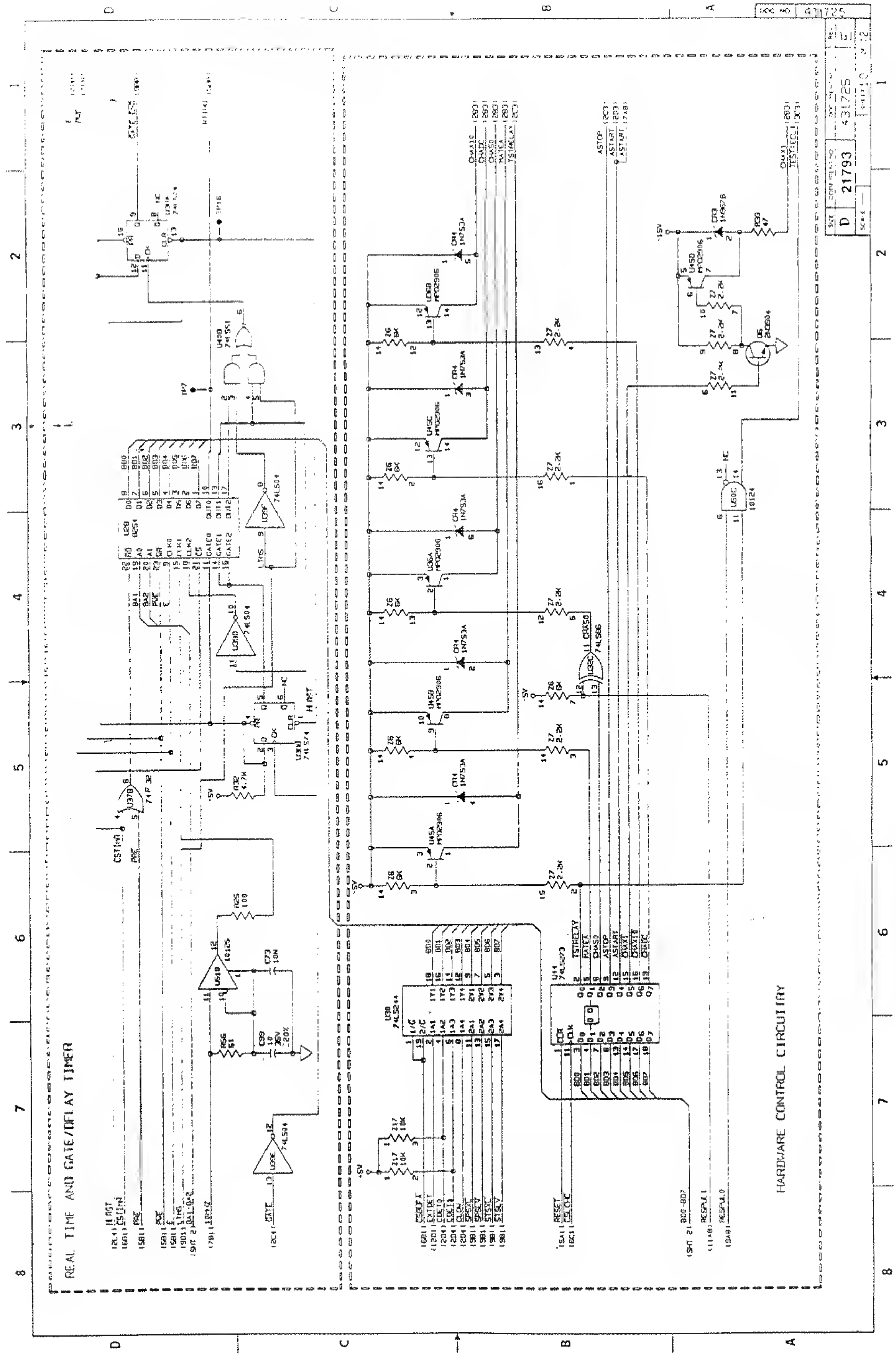


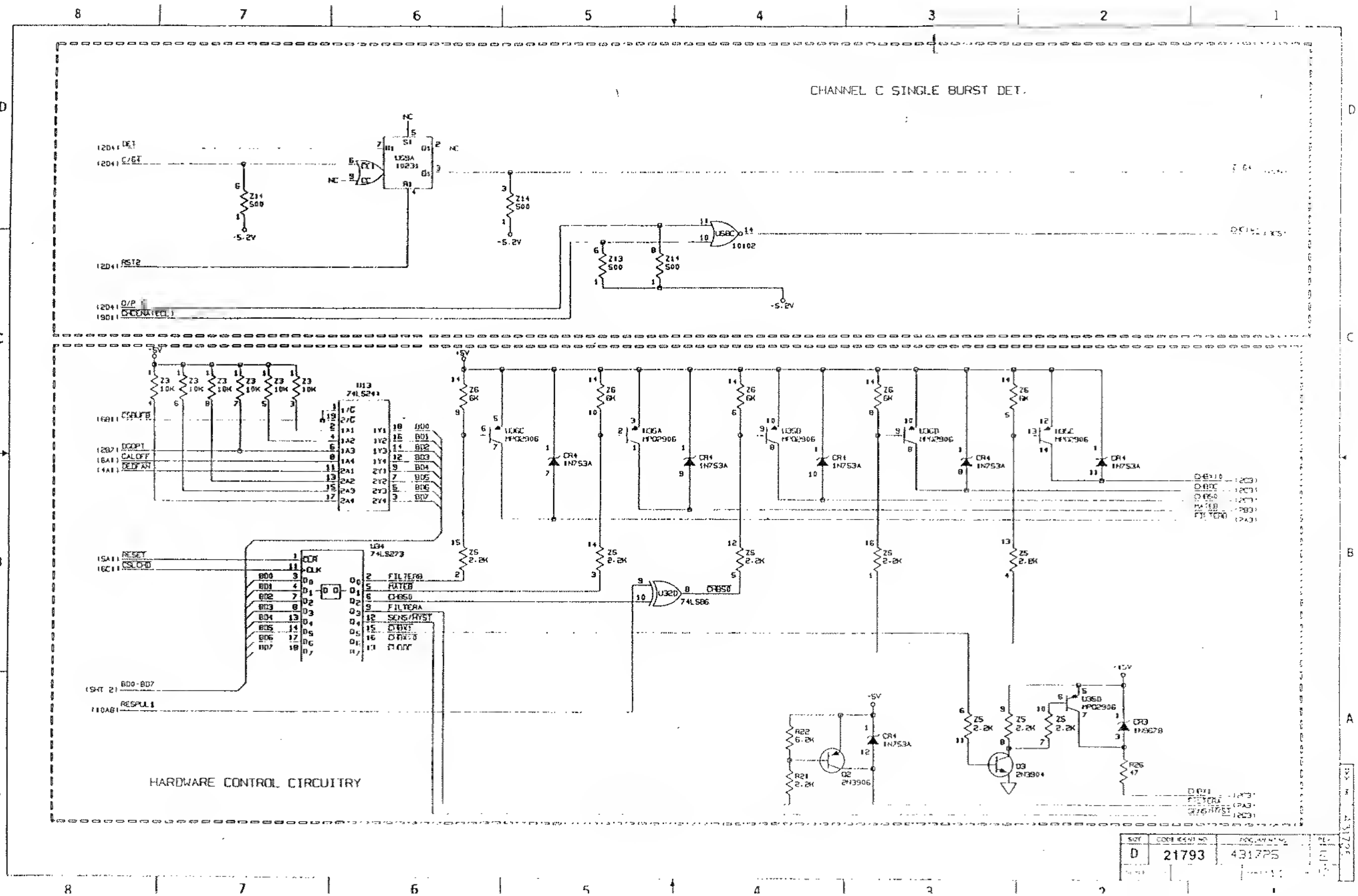
GPIB
START DAC
STOP DAC
REF. BUFFER
START AND STOP
TRIGGER LED STRETCH
CIRCUITRY
EXT/INT
REF. SELECT
21793

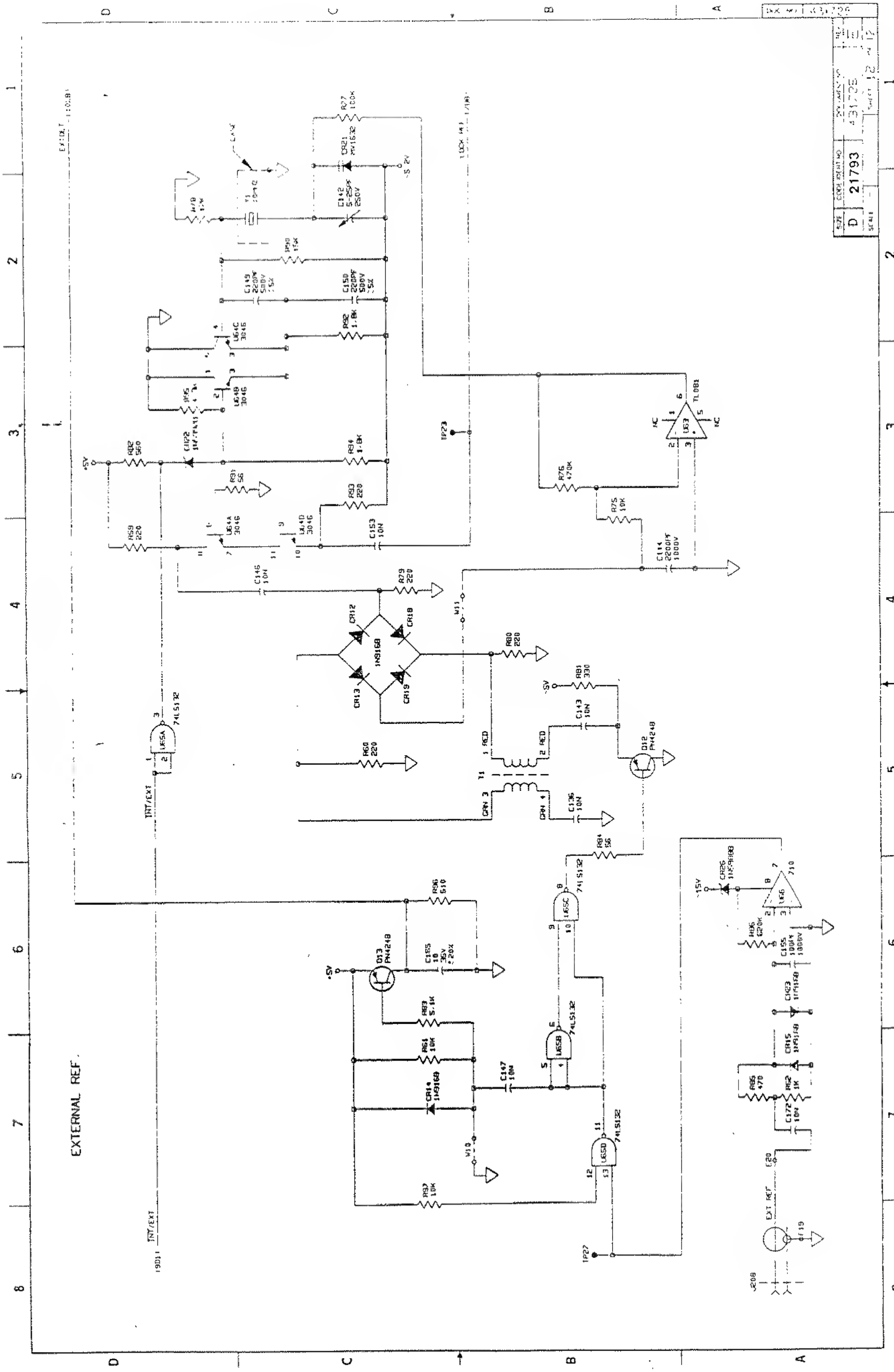

START AND STOP SIGNAL BUFFER
CHANNEL D
SIGNAL CONDITIONER
431725
21793

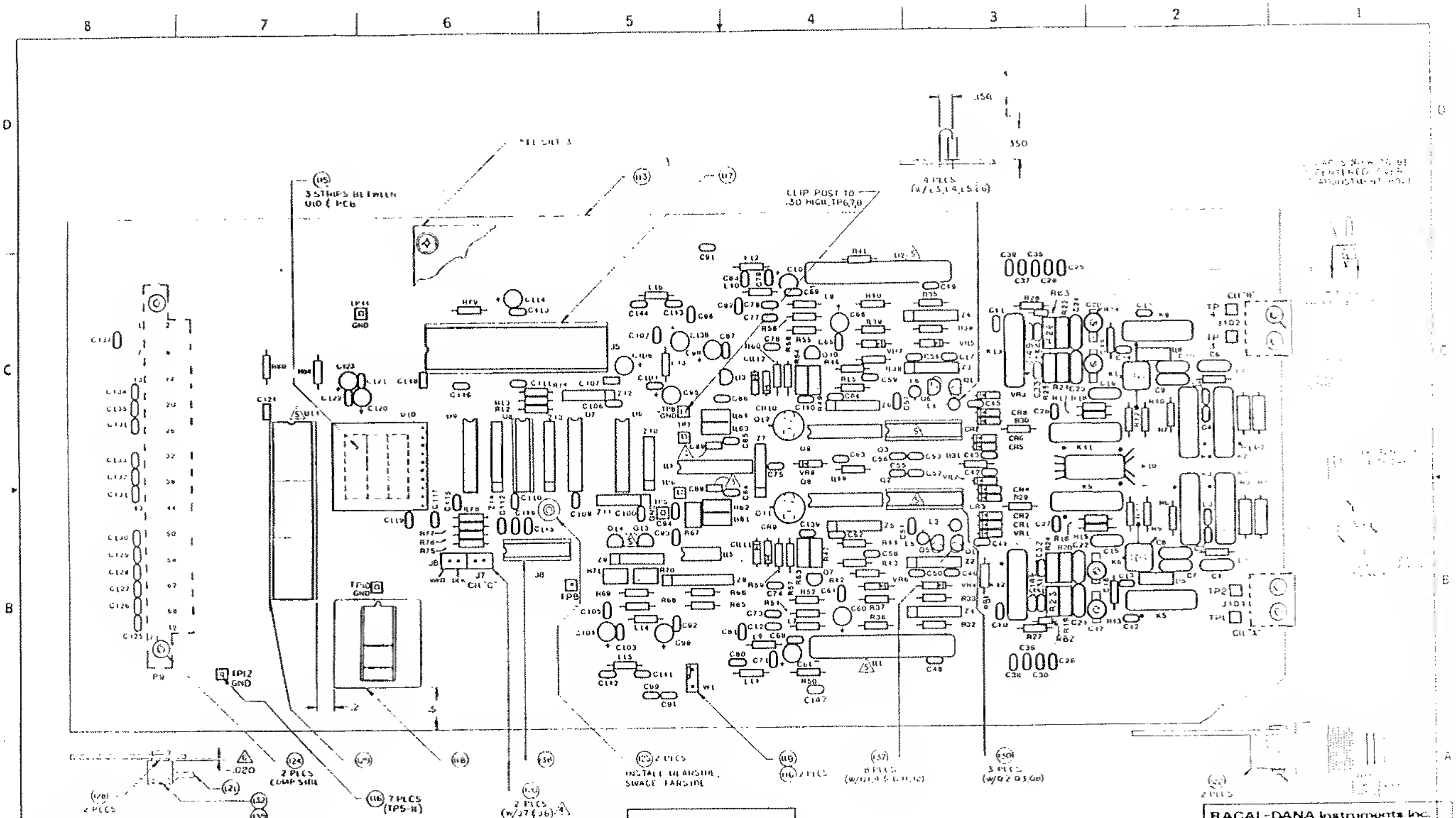


HARDWARE CONTROL CIRCUITRY
EXT. ARMING AND GATING CIRCUITRY
STOP ENABLE SELECT (SPEN)
AUTO TRIGGER CIRCUITRY
D
21793
431725


REAL TIME AND GATE/DELAY TIMER
HARDWARE CONTROL CIRCUITRY
D
21793
431725


CHANNEL C SINGLE BURST DET.
HARDWARE CONTROL CIRCUITRY
U13
74LS241
U34
74LS273
U32D
74LS86
U58C
10102
U59A
10231
DET
C/GT
RST2
O/P
CHCENA(ECL)
CBAUFB
DCOPT
CALOFF
DEDFAN
RESET
CSLCHD
BD0-BD7
RESPUL1
FILTERB
RATEB
CHBSD
FILTERA
SENS/RYST
Z3 10K
Z6 6K
Z5 2.2K
Z13 500
Z14 500
CR4 1N753A
MPQ2906
Q3 2N3904
Q2 2N3906
R22 6.2K
R21 2.2K
R26 47
+5V
-5.2V
D
21793
4317P5


EXTERNAL REF.
D
21793



1. Q2 Q3 Q13 Q14,U1,U2,U11 ARE STATIC SENSITIVE DEVICES.
2. INSTALL WITH SHORT PIN IN PCB
3. SOLDER C88,C89 TO PADS ON COMP CIRCUIT SIDE OF PCB.
4. AREA SHOWN MUST BE SMOOTH & FLAT AFTER SOLDER PROCESS IS COMPLETE. (MASK DURING WAVE SOLDER)
5. MAINTAIN .020 CLEARANCE ALONG ENTIRE LENGTH BETWEEN COMN & PCB.

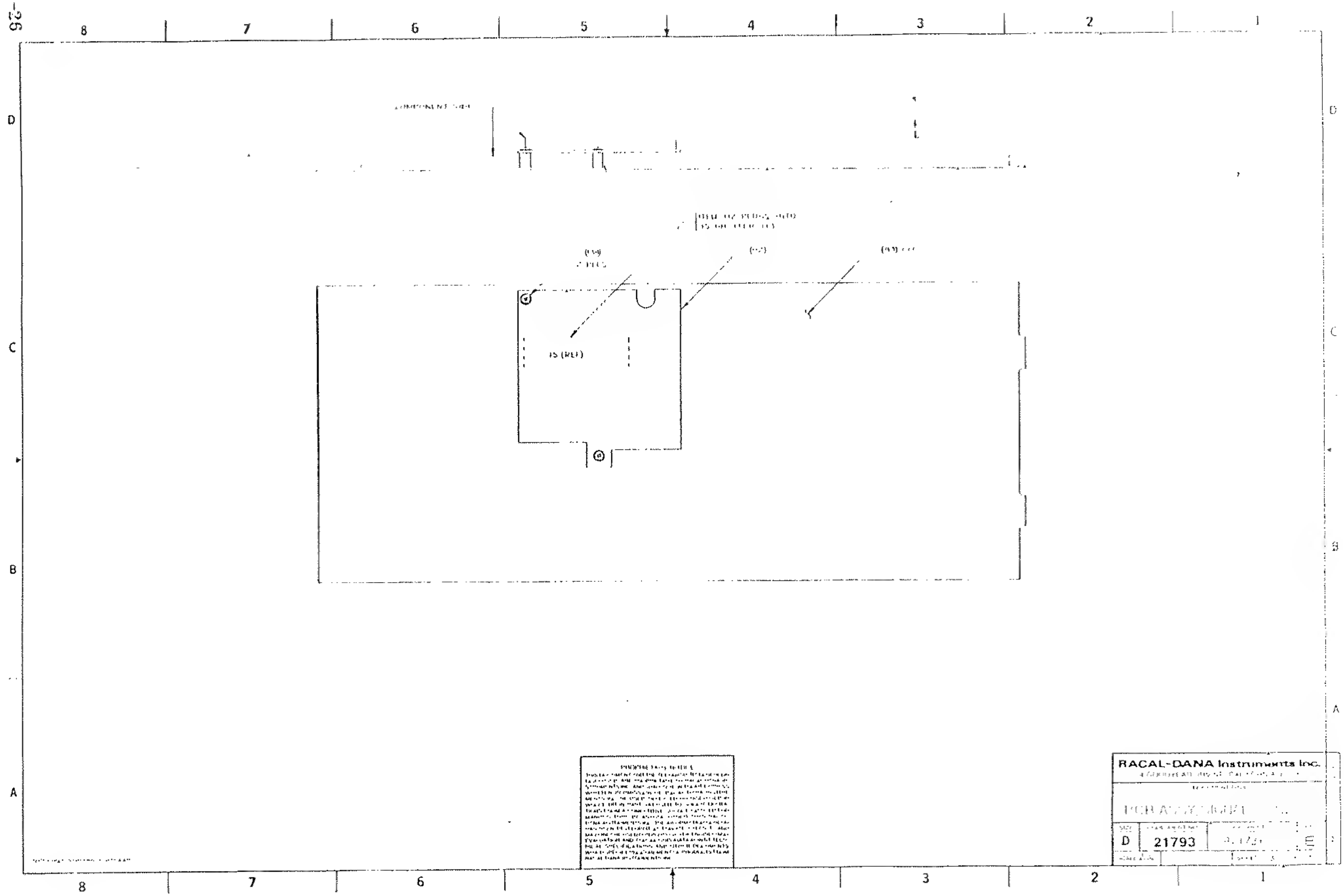
1 REF SCHEMATIC

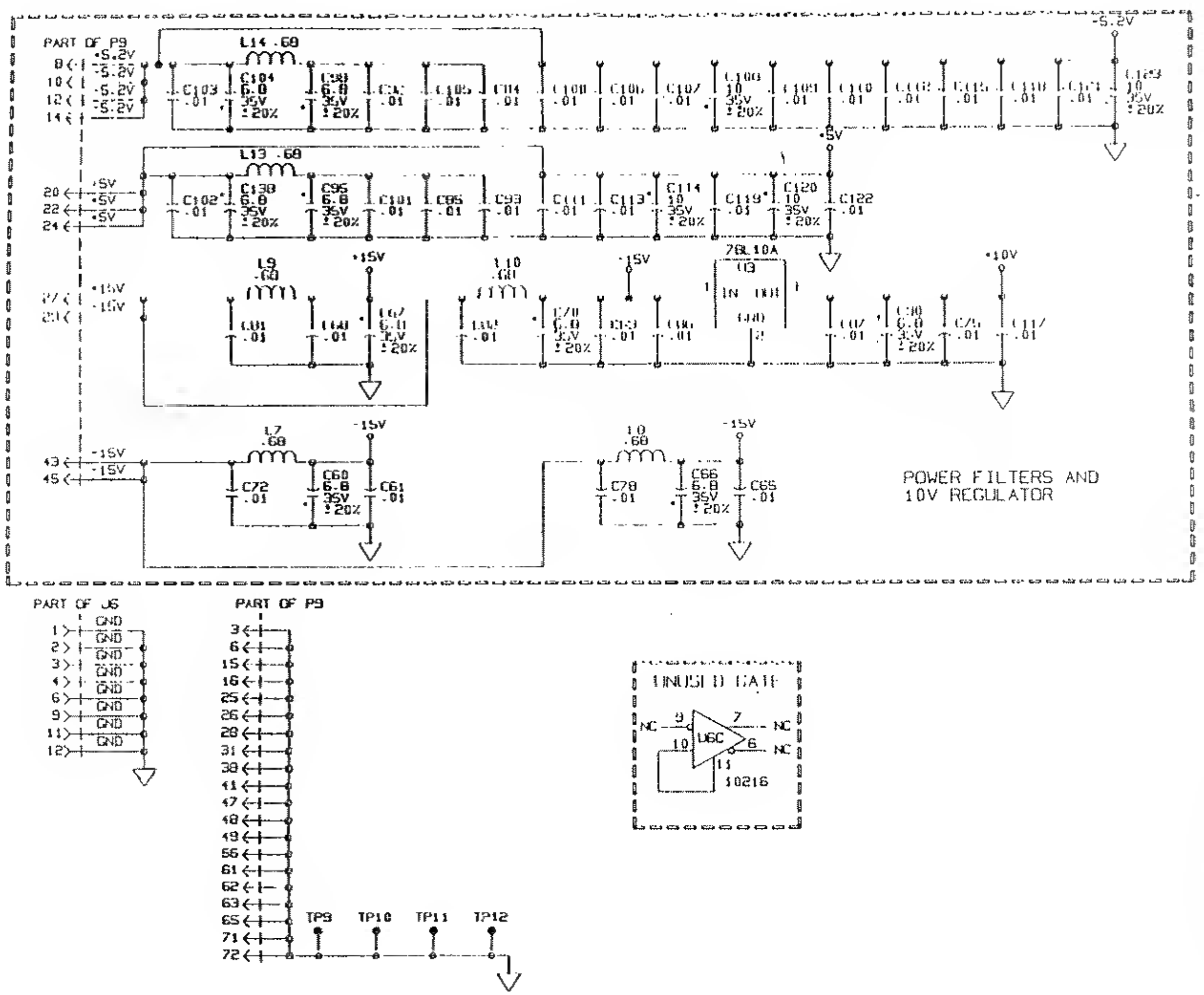
RACAL-DANA Instruments Inc.

PCB ASSEMBLY

D 21793

7-26





Z14	Z11	
W1		
VR8		
U11		
TP12		
R84		
Q14		
P9		
L16		
K13		
J102		
CR12		
C149		
HIGHEST	NOT USED	
REF. DESIGNATIONS		

Z13	330	4 5	
Z10	330	4	
Z7	33	4	
Z6	330	4	
Z5	330	4	
Z4	2.2K	5 6	[illegible]
Z3	470	3 4	[illegible]
Z2	470	3 4	[illegible]
Z1	2.2K	[illegible]	[illegible]
Q9	[illegible]	[illegible]	
Q8	[illegible]	[illegible]	
REF. DES.	TYPE	[illegible]	

REF. DES.	IC TYPE	+5V PIN.NO.	+10V PIN.NO.	+15V PIN.NO.	GND PIN.NO.	-5.2V PIN.NO.	-15V PIN.NO.
J5	CONNECTOR	10.29.31			11.21.30. 35.40	1 20	
Q8.9	SL3127C				5		
Q2.3	SD5000N						2 15
U11	MCC1				16.36		
U10	1034	2	3		7.9	5	
U8	10231				1.16	8	
U7	10H158				16	8	
U6.9	10216				1.16	8	
U5	2903	8					4
U4	9687	11			3.14	6	
U1.2	230753	15			7.14		1

IC POWER CONNECTIONS

4. CAPACITOR VALUES ARE IN MICROFARADS. ±10%.100V UNLESS OTHERWISE SPECIFIED.
3. RESISTOR VALUES ARE IN OHMS. ±1%.1/4W UNLESS OTHERWISE SPECIFIED.
2. RESISTOR NETWORKS ±2%.
1. CHOKES ARE IN MICROHENRYS ±10%.

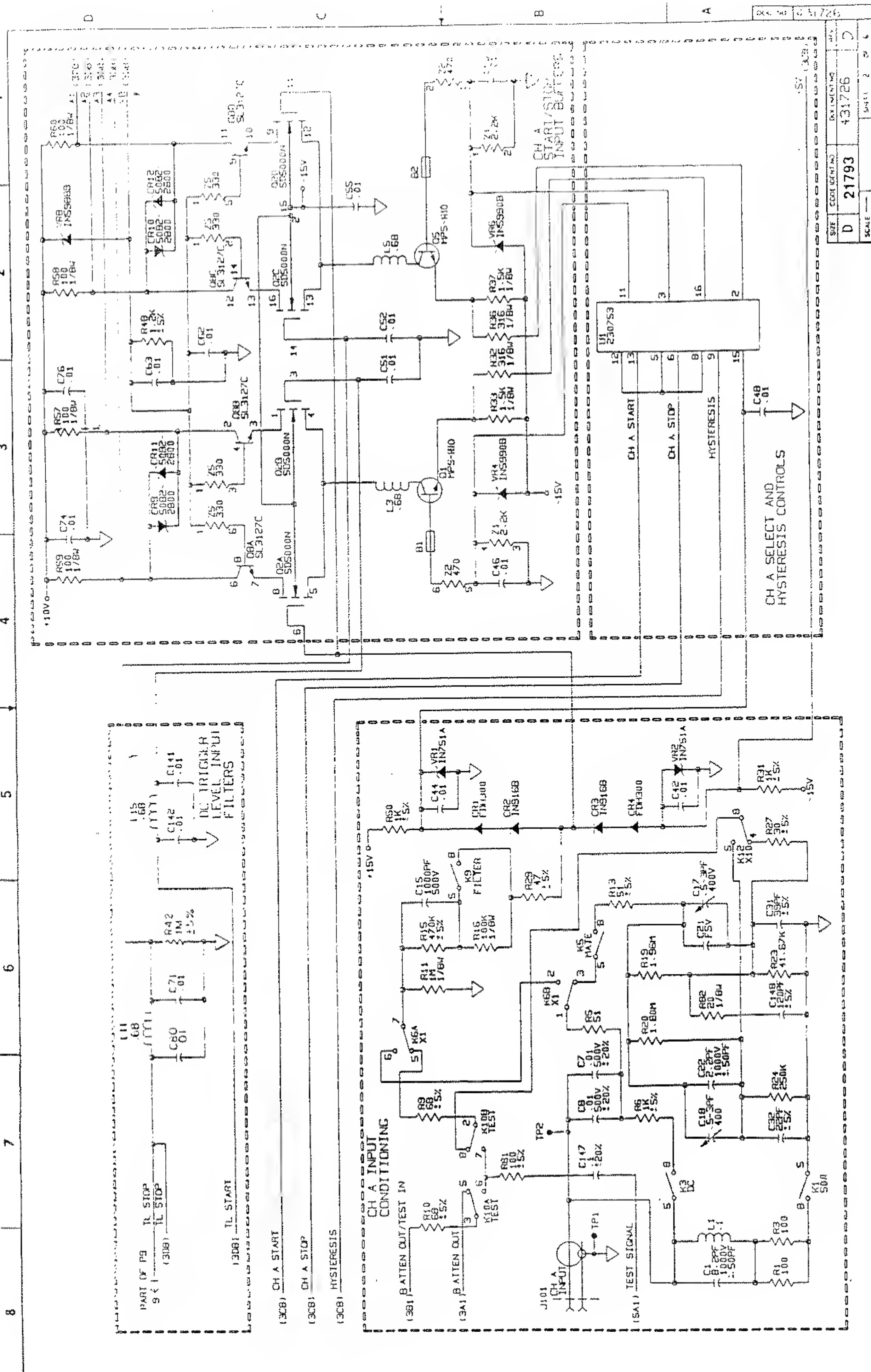
NOTES: UNLESS OTHERWISE SPECIFIED

PROPRIETARY NOTICE [illegible]

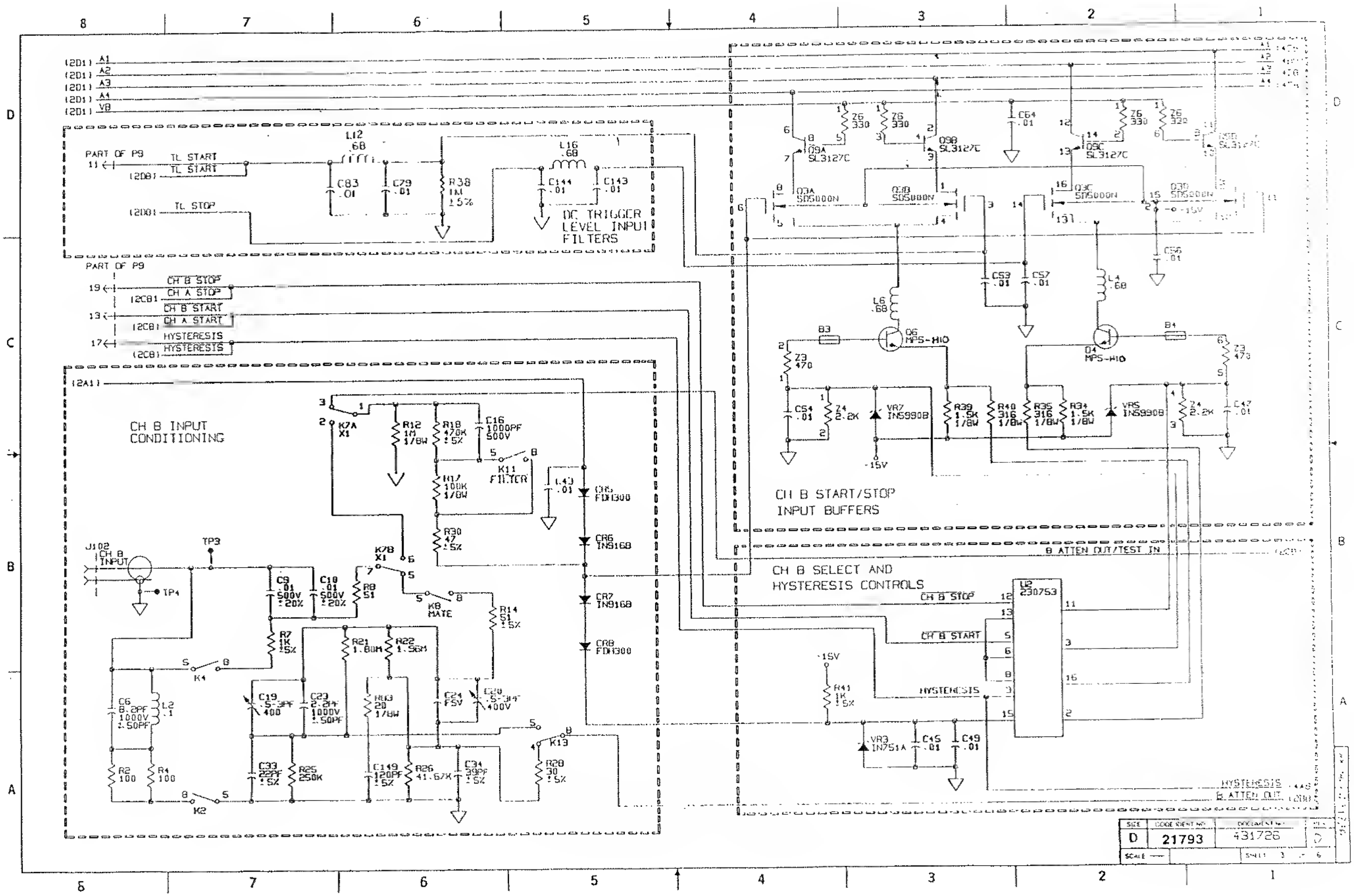
RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA [illegible]

SCHEM, SIGNAL COND

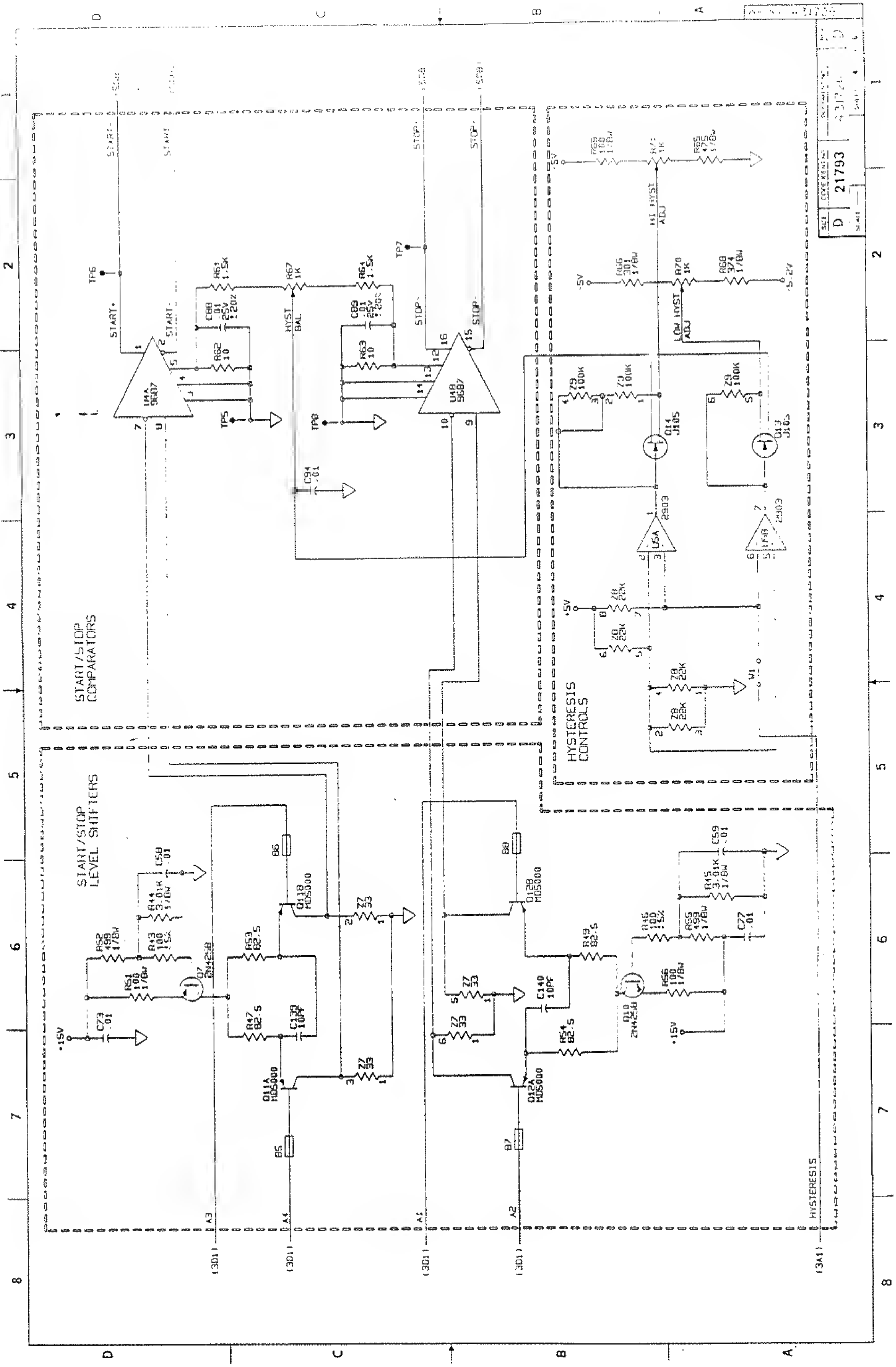
SIZE	CODE IDENT NO.		
D	21793	[illegible]	[illegible]

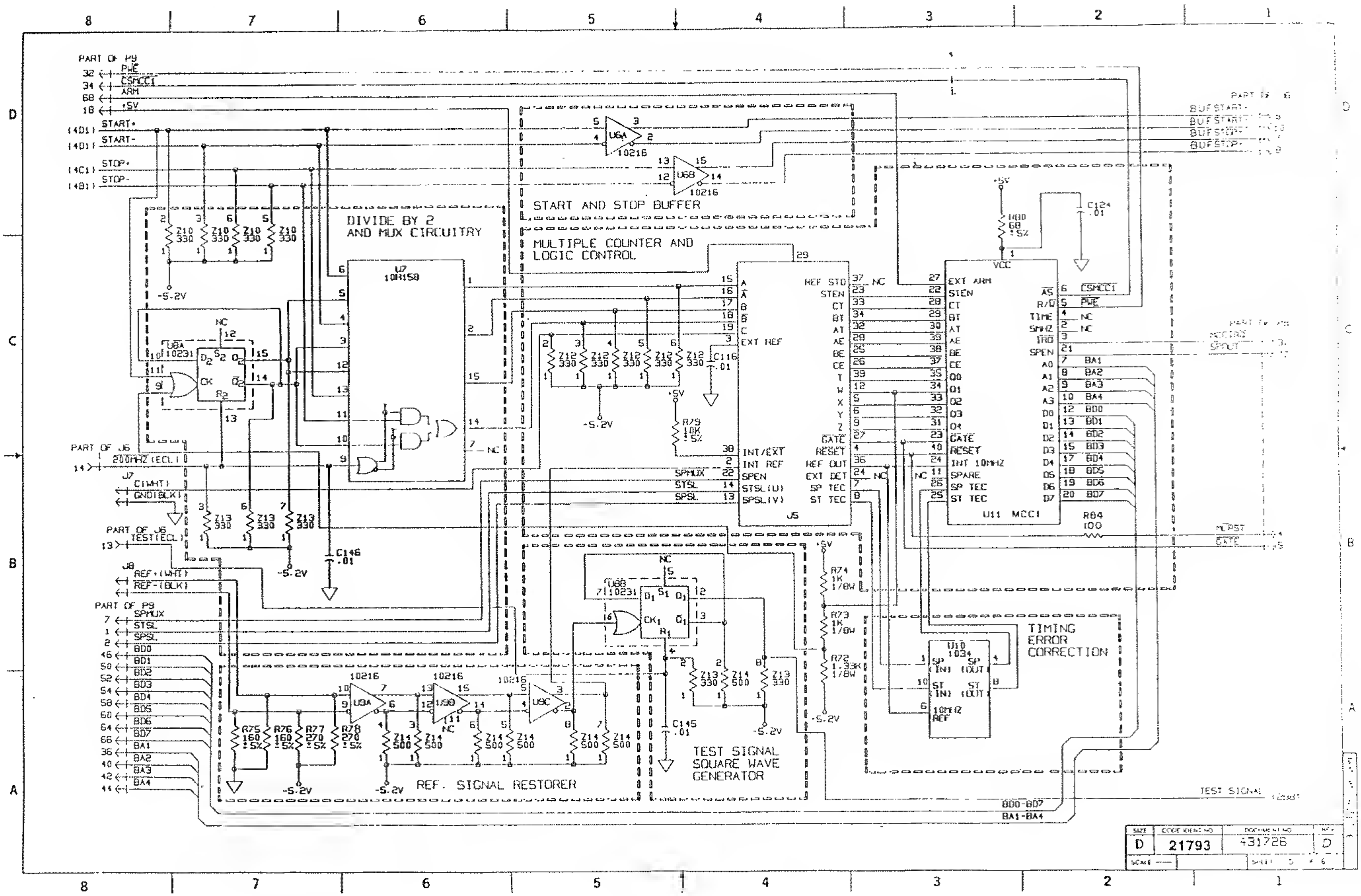


CH A SELECT AND
HYSTERESIS CONTROLS
CH A
START/STOP
INPUT BUFFERS
CH A INPUT
CONDITIONING
DC TRIGGER
LEVEL INPUT
FILTERS
CH A START
CH A STOP
HYSTERESIS
TL START
TL STOP
PART OF P3
ATTEN OUT/TEST IN
ATTEN OUT
TEST SIGNAL
J101
CH A
INPUT
TP1
TP2
K9
FILTER
K5
MATE
K3
DC
K1
50Ω
K10A
TEST
K10B
TEST
U1
230753
Q1
MPS-H10
Q5
MPS-H10
+10V
+15V
-15V
21793
431726

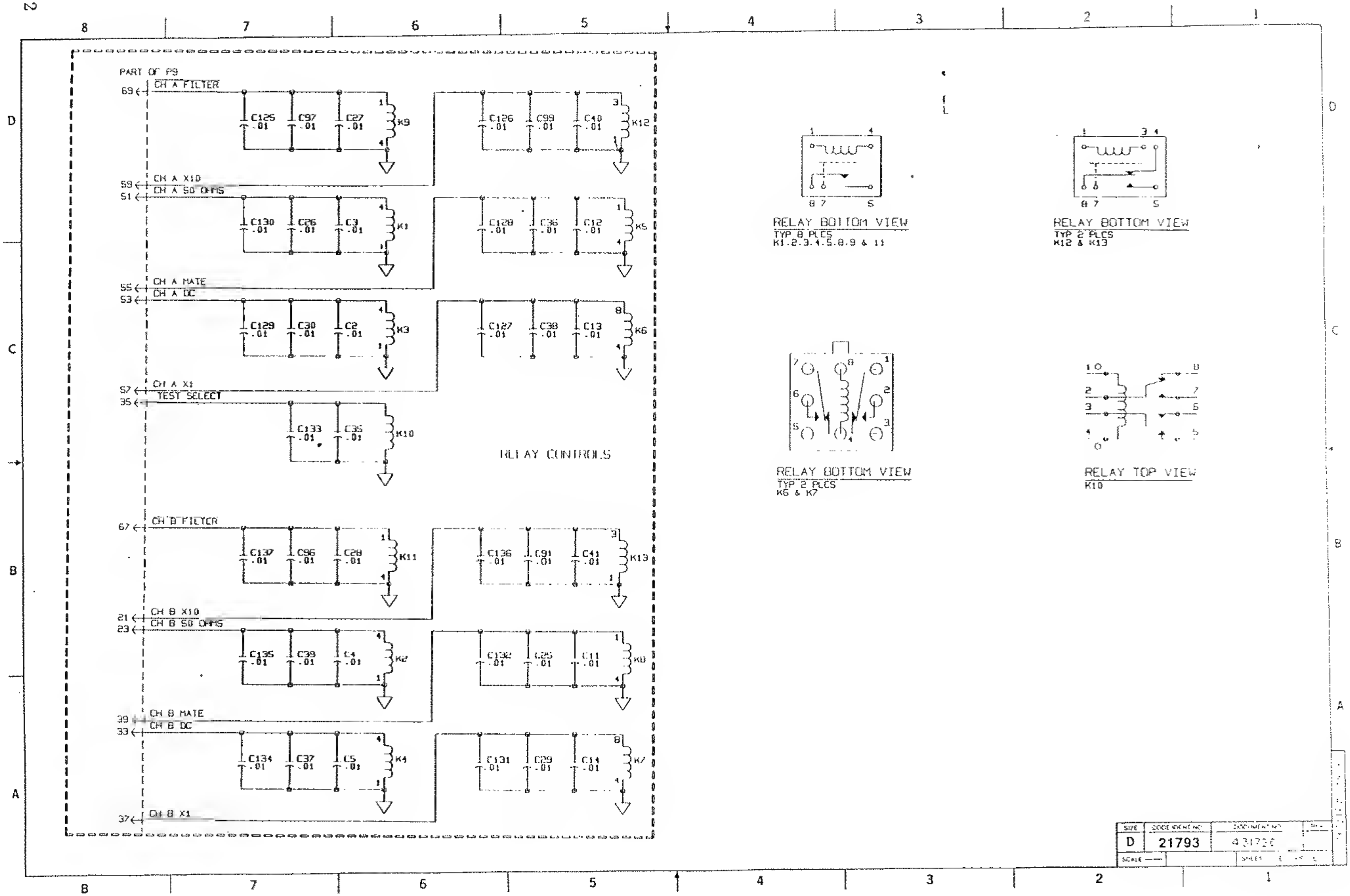


DC TRIGGER LEVEL INPUT FILTERS
PART OF P9
TL START
TL STOP
CH B STOP
CH A STOP
CH B START
CH A START
HYSTERESIS
CH B INPUT CONDITIONING
J102 CH B INPUT
TP3
TP4
K7A X1
K7B X1
K11 FILTER
K8 MATE
K4
K2
K13
CR5 FDH300
CR6 IN9168
CR7 IN9168
CR8 FDH300
CH B START/STOP INPUT BUFFERS
Q6 MPS-H10
Q4 MPS-H10
Q9A SL3127C
Q9B SL3127C
Q9C SL3127C
Q3A SD5000N
Q3B SD5000N
Q3C SD5000N
VR7 IN5908B
VR5 IN5908B
-15V
B ATTEN OUT/TEST IN
CH B SELECT AND HYSTERESIS CONTROLS
U2 230753
VR3 IN751A
HYSTERESIS
B ATTEN OUT
SIZE D
CODE IDENT NO. 21793
431726

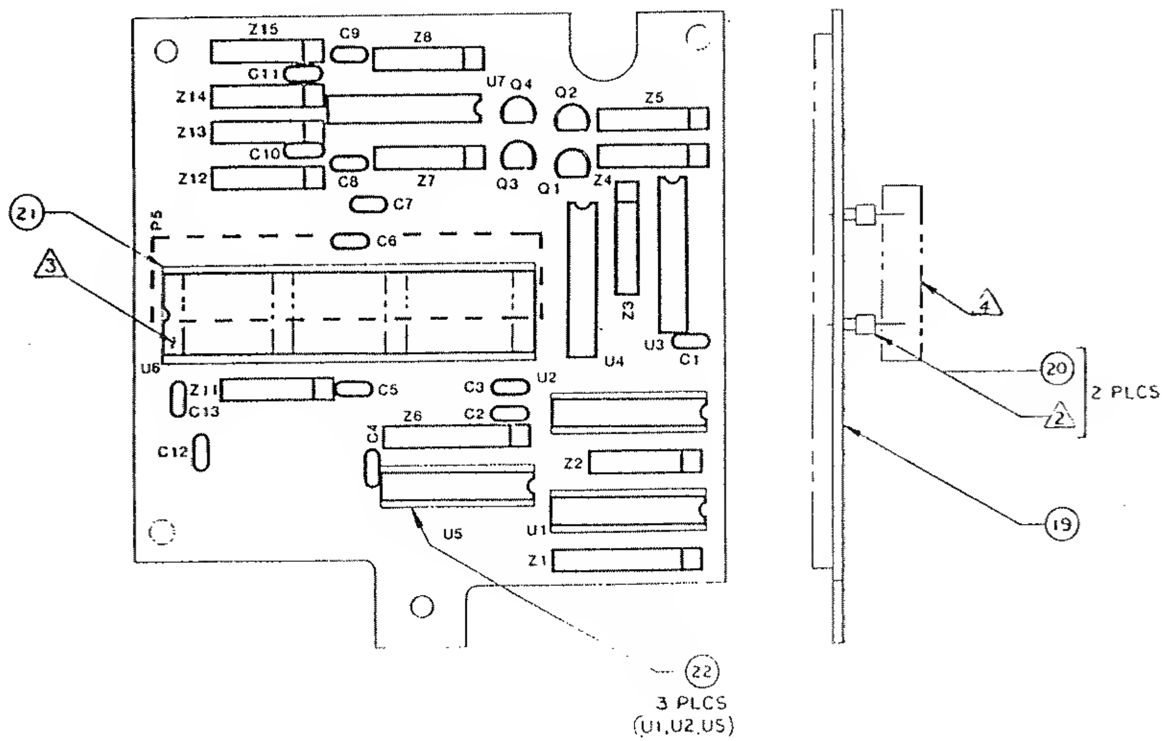

START/STOP COMPARATORS
START/STOP LEVEL SHIFTERS
HYSTERESIS CONTROLS
HYSTERESIS
HYST BAL
HI HYST ADJ
LOW HYST ADJ
21793



PART OF P9
START AND STOP BUFFER
MULTIPLE COUNTER AND
LOGIC CONTROL
DIVIDE BY 2
AND MUX CIRCUITRY
U7
10H158
J5
U11 MCC1
U10
1034
TIMING
ERROR
CORRECTION
TEST SIGNAL
SQUARE WAVE
GENERATOR
REF. SIGNAL RESTORER
PART OF J6
200MHZ (ECL)
PART OF J6
TEST (ECL)
BD0-BD7
BA1-BA4
TEST SIGNAL
D
21793
431726


PART OF P9
69 CH A FILTER
59 CH A X10
51 CH A 50 OHMS
55 CH A MATE
53 CH A DC
57 CH A X1
35 TEST SELECT
67 CH B FILTER
21 CH B X10
23 CH B 50 OHMS
39 CH B MATE
33 CH B DC
37 CH B X1
C125 .01
C97 .01
C27 .01
K9
C126 .01
C99 .01
C40 .01
K12
C130 .01
C26 .01
C3 .01
K1
C128 .01
C36 .01
C12 .01
K5
C129 .01
C30 .01
C2 .01
K3
C127 .01
C38 .01
C13 .01
K6
C133 .01
C35 .01
K10
RELAY CONTROLS
C137 .01
C96 .01
C28 .01
K11
C136 .01
C91 .01
C41 .01
K13
C135 .01
C39 .01
C4 .01
K2
C132 .01
C25 .01
C11 .01
K8
C134 .01
C37 .01
C5 .01
K4
C131 .01
C29 .01
C14 .01
K7
RELAY BOTTOM VIEW
TYP 8 PLCS
K1,2,3,4,5,8,9 & 11
RELAY BOTTOM VIEW
TYP 2 PLCS
K12 & K13
RELAY BOTTOM VIEW
TYP 2 PLCS
K6 & K7
RELAY TOP VIEW
K10
SIZE
D
CODE IDENT NO
21793
DOCUMENT NO
431726

NOTES UNLESS OTHERWISE SPECIFIED



4 ITEM 20 PINS TO BE PROTECTED FROM DAMAGE DURING HANDLING AND STORAGE USING FOAM PAD. (REF. P/N 454754)

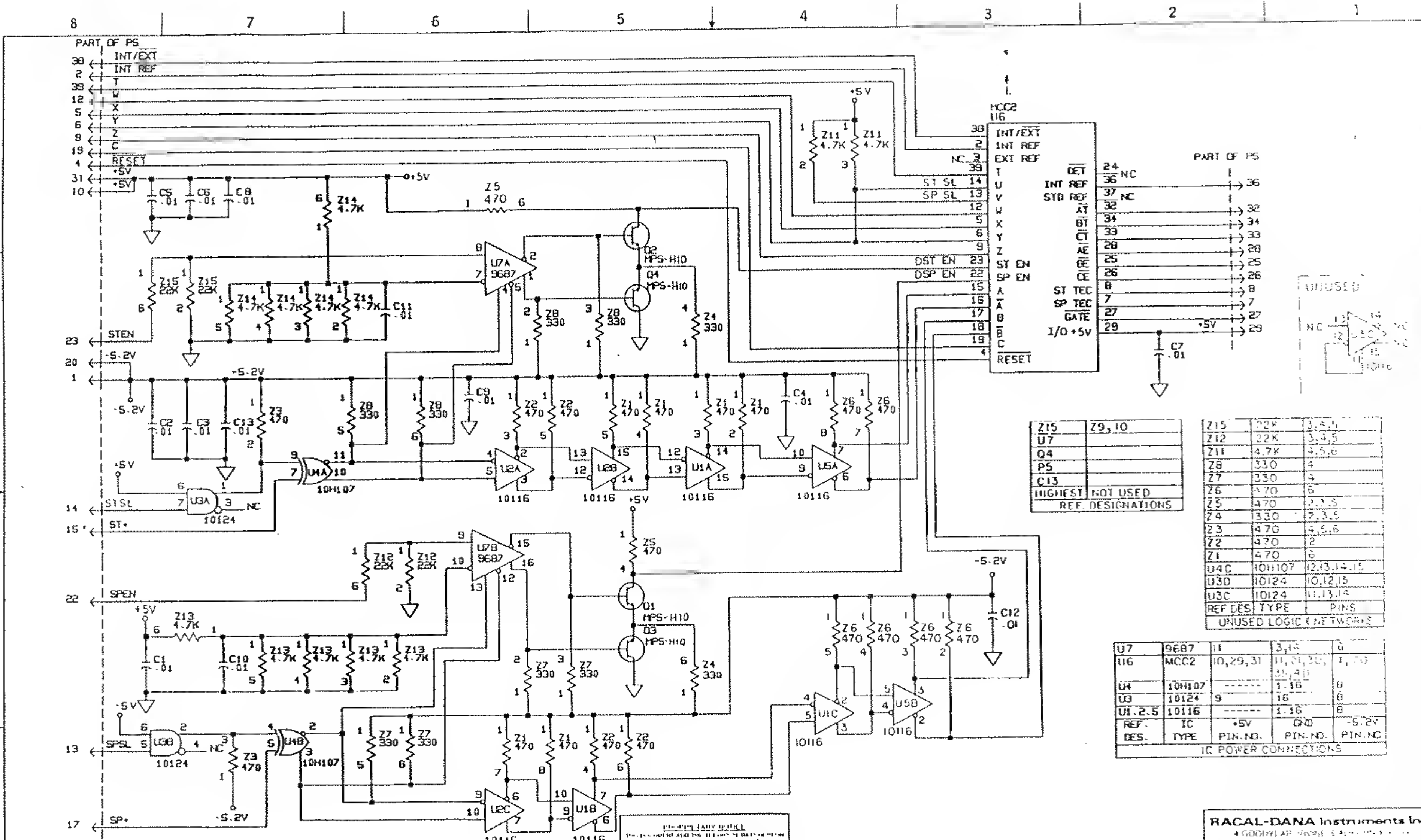
3 CROSS BARS ON ITEM 21 TO BE CLIPPED FLUSH TO SOCKET SIDES AFTER WAVE SOLDER.

2 ITEM NO. 20 TO BE PERPENDICULAR AND FIRMLY SEATED ON PCB.

1. REF. SCHEMATIC 431728.

PCB ASSY, AMCC2 SYNTH		
C	21793	401728

SCALE NONE



Z15	Z9, 10
U7	
Q4	
P5	
C13	
HIGHEST	NOT USED
REF. DESIGNATIONS	

Z15	22K	3,4,5
Z12	22K	3,4,5
Z11	4.7K	4,5,6
Z8	330	4
Z7	330	4
Z6	470	6
Z5	470	2,3,5
Z4	330	2,3,5
Z3	470	4,5,6
Z2	470	2
Z1	470	6
U4C	10H107	12,13,14,15
U3D	10124	10,12,15
U3C	10124	11,13,14
REF DES	TYPE	PINS
UNUSED LOGIC & NETWORKS		

U7	9687	11	3,13	6
U6	MCC2	10,29,31	11,21,30, 35,40	1,20
U4	10H107	------	1,16	8
U3	10124	9	16	8
U1,2,5	10116	------	1,16	8
REF. DES.	IC TYPE	+5V PIN.NO.	GND PIN.NO.	-5.2V PIN.NO.
IC POWER CONNECTIONS				

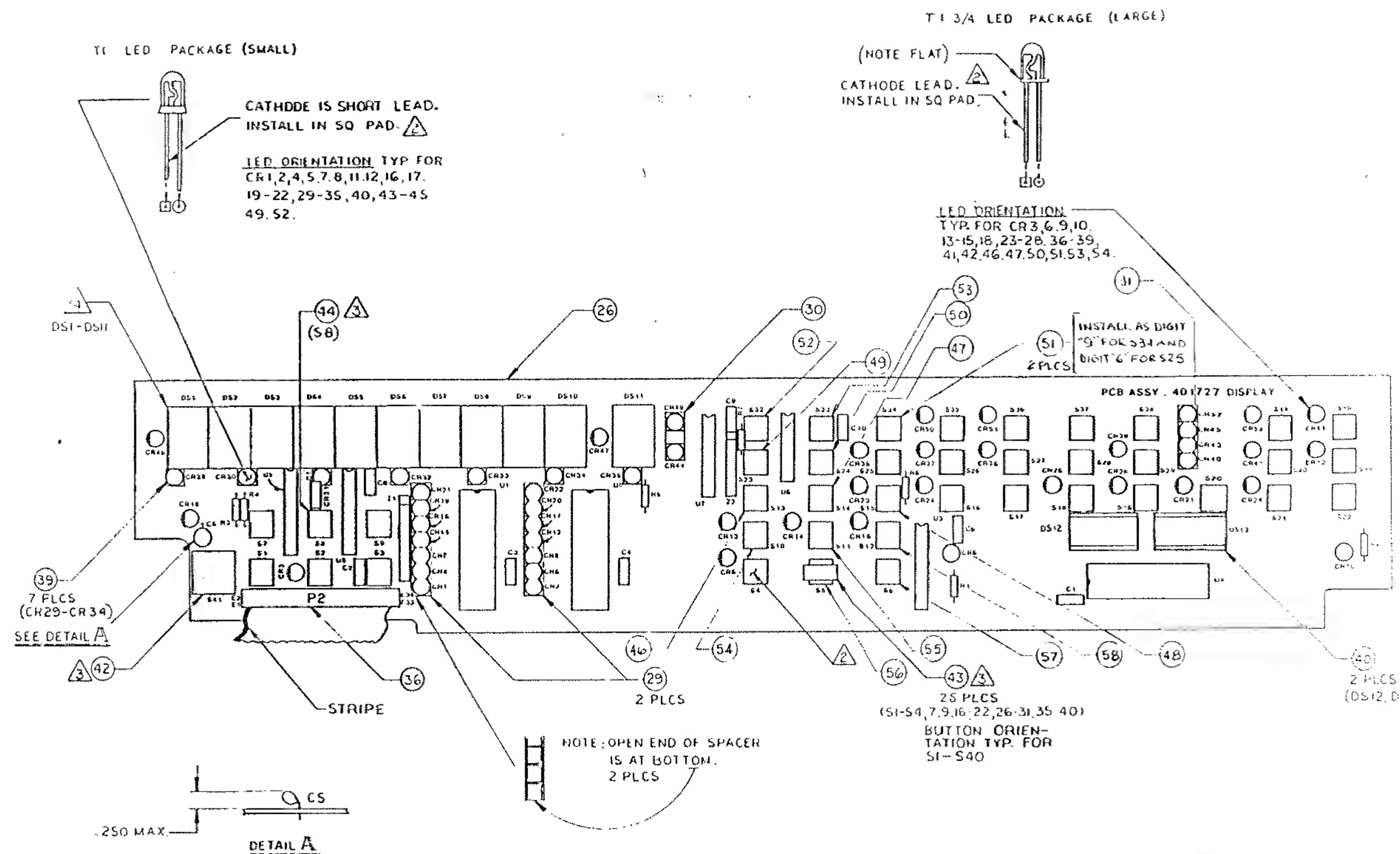
3. CAPACITOR VALUES ARE IN MICROFARIDS, ±10%, 100V UNLESS OTHERWISE SPECIFIED.
2. RESISTOR VALUES ARE IN OHMS.
1. ALL RESISTOR NETWORKS ±2%.

NOTES UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc.

SCHEM, MCC2 SYNCH.

SIZE	CODE IDENT NO.	
D	21793	431728



4 DS1-DS11 TO BE INSTALLED USING THE SAME INTENSITY CODE.

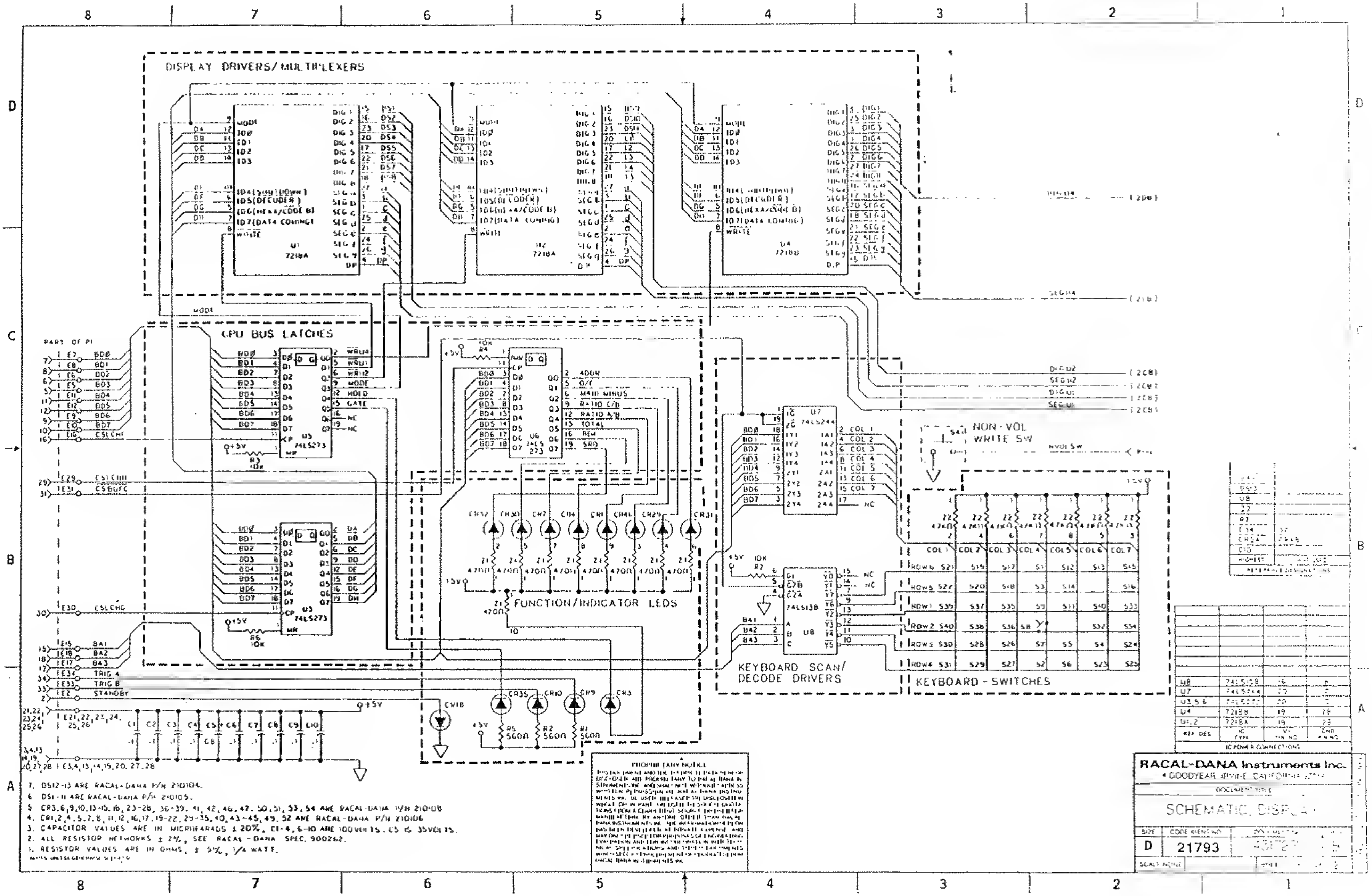
3 ENSURE BUTTON IS FIRMLY SEATED ON SWITCH.

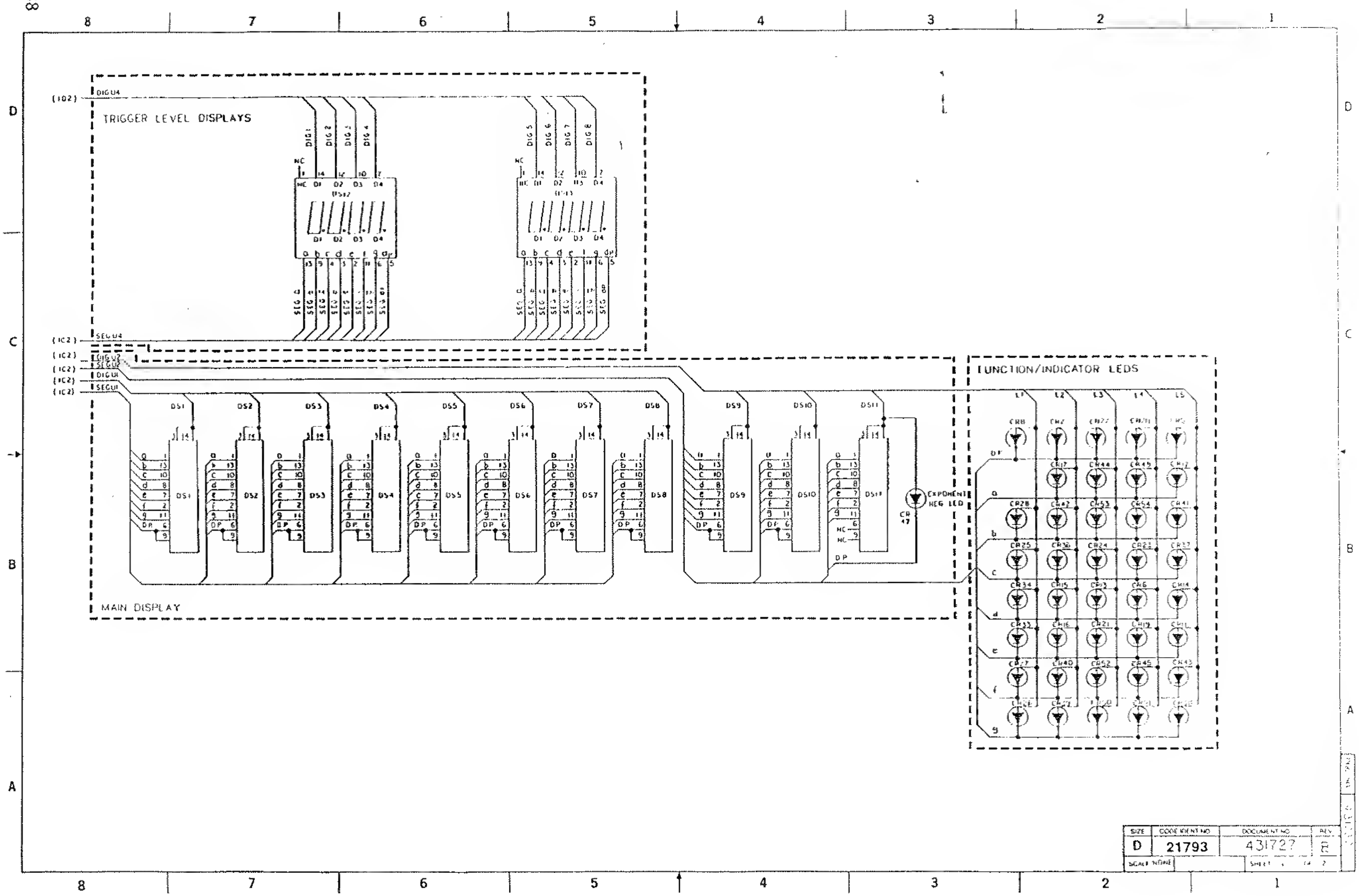
2 INSTALL ALL LEDS (CR1-47,49-54) AND SWITCHES (S1-41) FLUSH TO PCB.

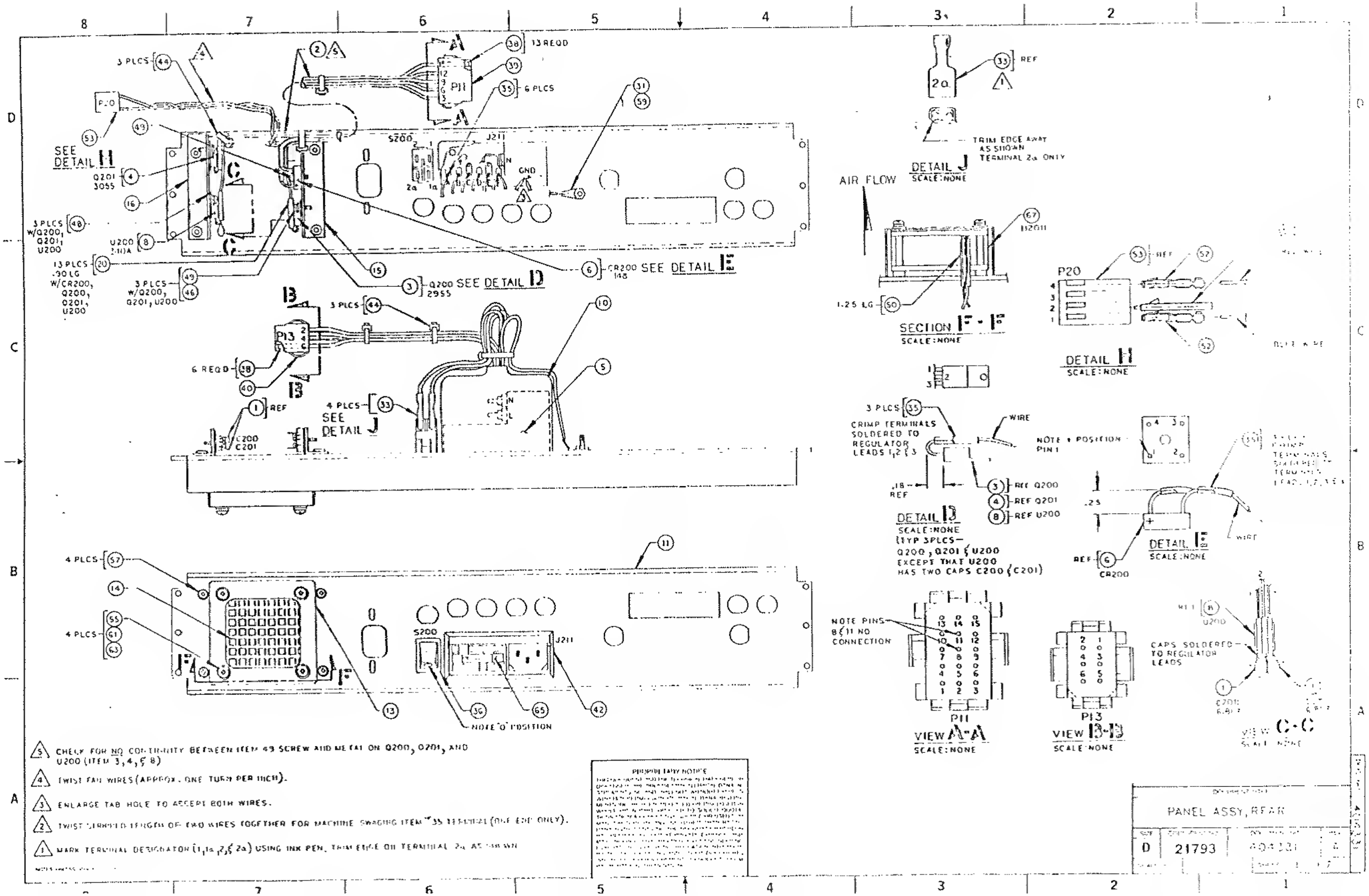
1. REF. SCH. 431727.

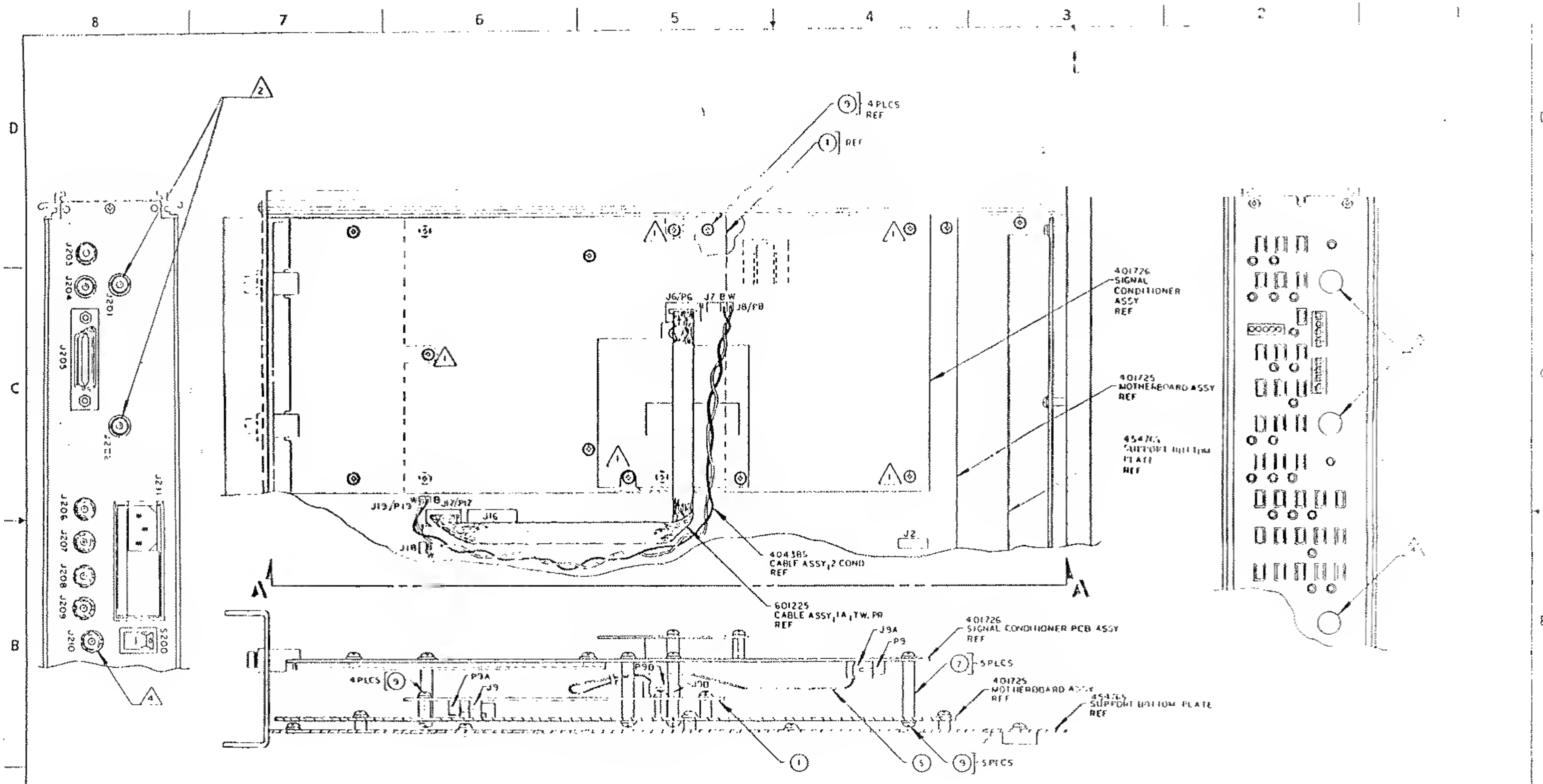
NOTES UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc. 4 GOODYEAR, IRVINE, CALIFORNIA 92714			
DOCUMENT TITLE: PCB ASSY, DISPLAY			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	401727	-
SCALE NONE		SHEET 1 OF 3	


DISPLAY DRIVERS/MULTIPLEXERS
CPU BUS LATCHES
FUNCTION/INDICATOR LEDS
KEYBOARD SCAN/
DECODE DRIVERS
KEYBOARD - SWITCHES
NON-VOL
WRITE SW
PART OF P1
7. DS12-13 ARE RACAL-DANA P/N 210104.
6. DS1-11 ARE RACAL-DANA P/N 210105.
5. CR3,6,9,10,13-15,16,23-28,30-39,41,42,46,47,50,51,53,54 ARE RACAL-DANA P/N 210108
4. CR1,2,4,5,7,8,11,12,16,17,19-22,29-35,40,43-45,49,52 ARE RACAL-DANA P/N 210106
3. CAPACITOR VALUES ARE IN MICROFARADS ±20%, C1-4,6-10 ARE 100VOLTS, C5 IS 35VOLTS.
2. ALL RESISTOR NETWORKS ± 2%, SEE RACAL-DANA SPEC. 900262.
1. RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 WATT.
NOTES UNLESS OTHERWISE SPECIFIED
PROPRIETARY NOTICE
IC POWER CONNECTIONS
RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA
SCHEMATIC, DISPLAY
D
21793


TRIGGER LEVEL DISPLAYS
MAIN DISPLAY
FUNCTION/INDICATOR LEDS
EXPONENT NEG LED
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
DS11
DS12
DIG 1
DIG 2
DIG 3
DIG 4
DIG 5
DIG 6
DIG 7
DIG 8
SIZE D
CODE IDENT NO 21793
DOCUMENT NO 431727
SCALE NONE


SEE DETAIL H
Q201 3055
U200 340A
3 PLCS W/Q200, Q201, U200
13 PLCS .90 LG W/CR200, Q200, Q201, U200
3 PLCS W/Q200, Q201, U200
P20
P11
13 REQD
6 PLCS
S200
J211
GND
CR200 148 SEE DETAIL E
Q200 2955 SEE DETAIL D
P13
6 REQD
REF
C200 C201
SEE DETAIL J
4 PLCS
3 PLCS
NOTE "O" POSITION
TRIM EDGE AWAY AS SHOWN TERMINAL 2a ONLY
DETAIL J
SCALE: NONE
AIR FLOW
SECTION F-F
SCALE: NONE
1.25 LG
U201
DETAIL H
SCALE: NONE
CRIMP TERMINALS SOLDERED TO REGULATOR LEADS 1, 2 & 3
WIRE
NOTE + POSITION PIN 1
REF Q200
REF Q201
REF U200
.18 REF
.25
DETAIL D
SCALE: NONE
(TYP 3PLCS–Q200, Q201 & U200 EXCEPT THAT U200 HAS TWO CAPS C200 & C201)
REF CR200
DETAIL E
SCALE: NONE
NOTE PINS 8 & 11 NO CONNECTION
P11
VIEW A-A
SCALE: NONE
P13
VIEW B-B
SCALE: NONE
CAPS SOLDERED TO REGULATOR LEADS
U200
C201
VIEW C-C
SCALE: NONE
5 CHECK FOR NO CONTINUITY BETWEEN ITEM 49 SCREW AND METAL ON Q200, Q201, AND U200 (ITEM 3, 4, & 8)
4 TWIST FAN WIRES (APPROX. ONE TURN PER INCH).
3 ENLARGE TAB HOLE TO ACCEPT BOTH WIRES.
2 TWIST STRIPPED LENGTH OF TWO WIRES TOGETHER FOR MACHINE SWAGING ITEM 35 TERMINAL (ONE END ONLY).
1 MARK TERMINAL DESIGNATOR (1, 1a, 2, & 2a) USING INK PEN. TRIM EDGE ON TERMINAL 2a AS SHOWN
PROPRIETARY NOTICE
PANEL ASSY, REAR
D
21793



SECTION A-A

4. REMOVE CHANNEL C BNC FROM FRONT PANEL AND INSTALL IN REAR PANEL. ROUTE CABLE TO REAR PANEL (NO ATTACHMENTS REQD) MOVE HOLE PLUG FROM REAR PANEL TO FRONT PANEL. (REF. MODEL 1996 ONLY).

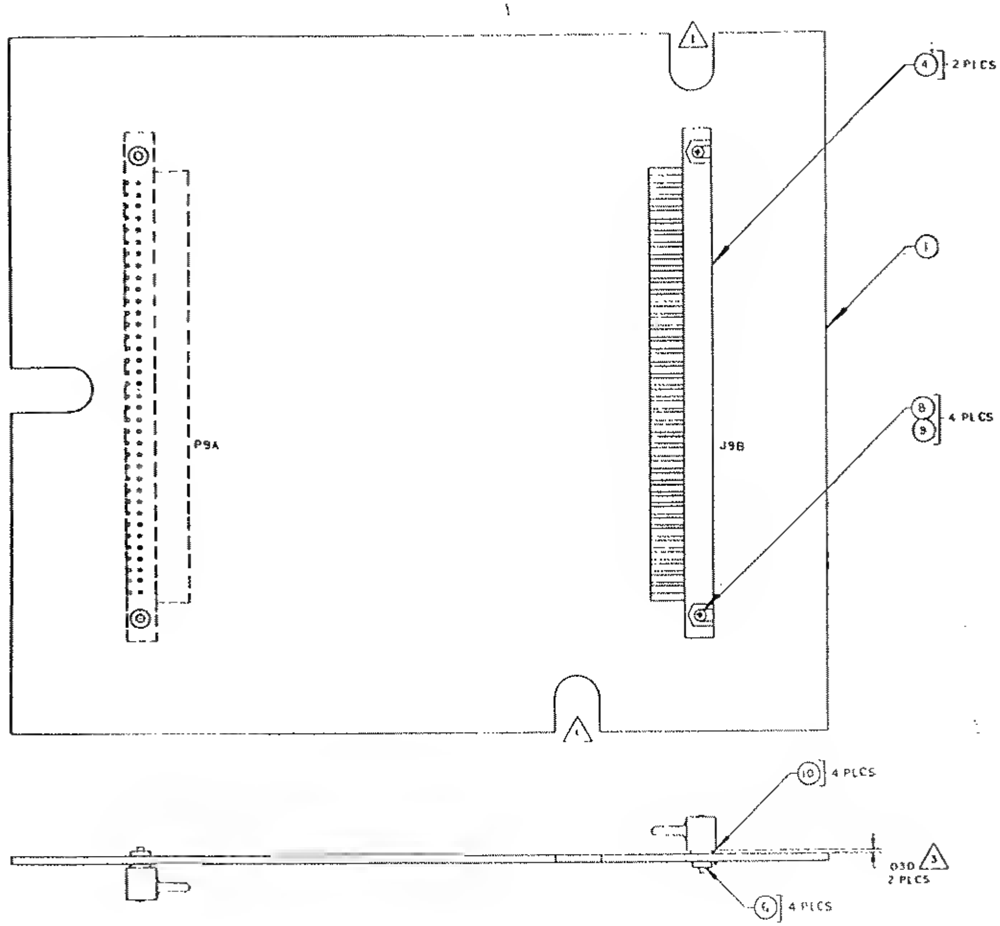
3. SHIFT PLASTIC PLUGS 610221 (SUPPLIED WITH TOP-LINE REF) FROM REAR PANEL TO RELATING HOLES IN FRONT PANEL. NOTE: ONLY APPLICABLE IF REAR INPUT IS INSTALLED AFTER OR DURING FINAL ASSY BUILD.

2. LOCK NUTS SUPPLIED WITH BNCS ON SIGNAL CONDITIONER.

1. SCREWS NOTED SUPPLIED WITH CHASSIS ASSY. WILL BE USED IN SAME POSITION. ON SIGNAL CONDITIONER AS IN STD FRONT INPUT CONFIG.

REAR INPUT ASSY, OPT. 01

D	21793	404378	A



3. MAINTAIN .030 CLEARANCE BETWEEN CONN (ITEM 8) & PCB TYP.

2. SCHEMATIC REF. 431752.

1. VERIFY ORIENTATION OF SLOTS PRIOR TO CONNECTOR INSTALLATION.

NOTES: UNLESS OTHERWISE SPECIFIED

PROPRIETARY NOTICE

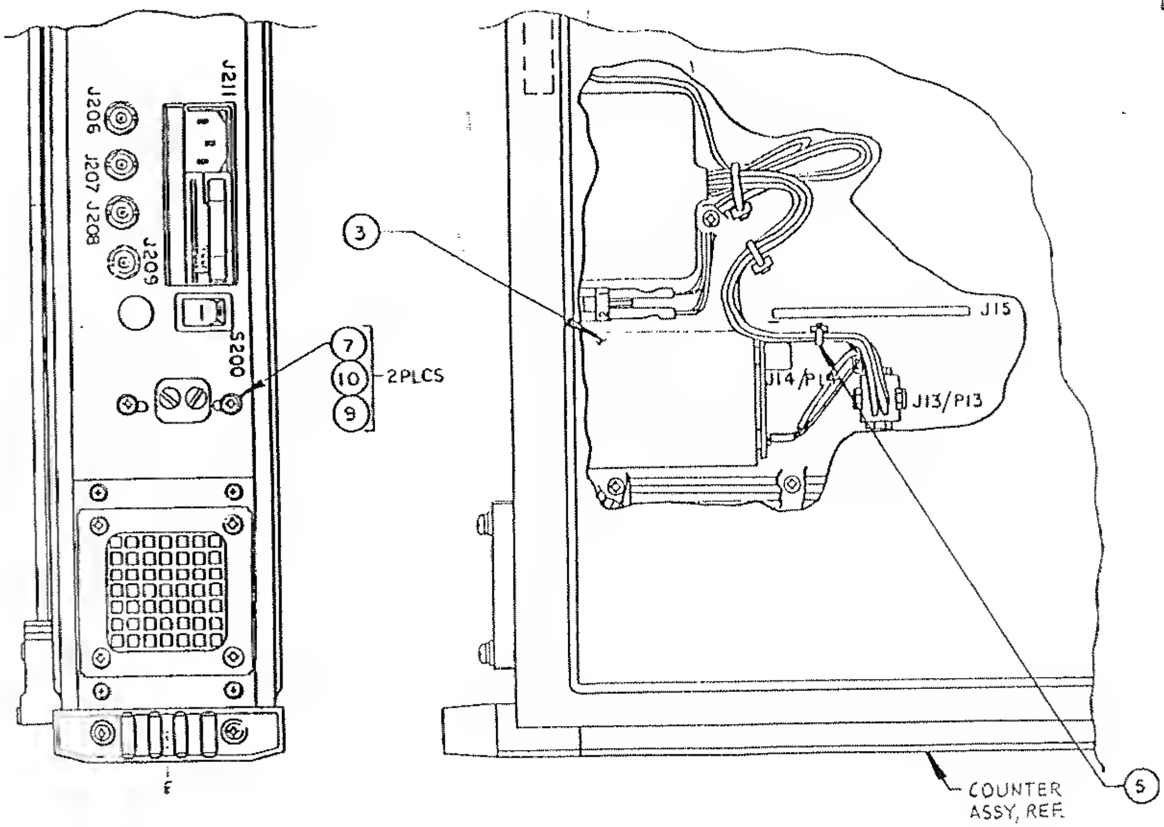
PCB ASSY, REAR INPUT

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	401752	2

SCALE 2/1 SHEET 1

DWG NO 401752

NOTES UNLESS OTHERWISE SPECIFIED

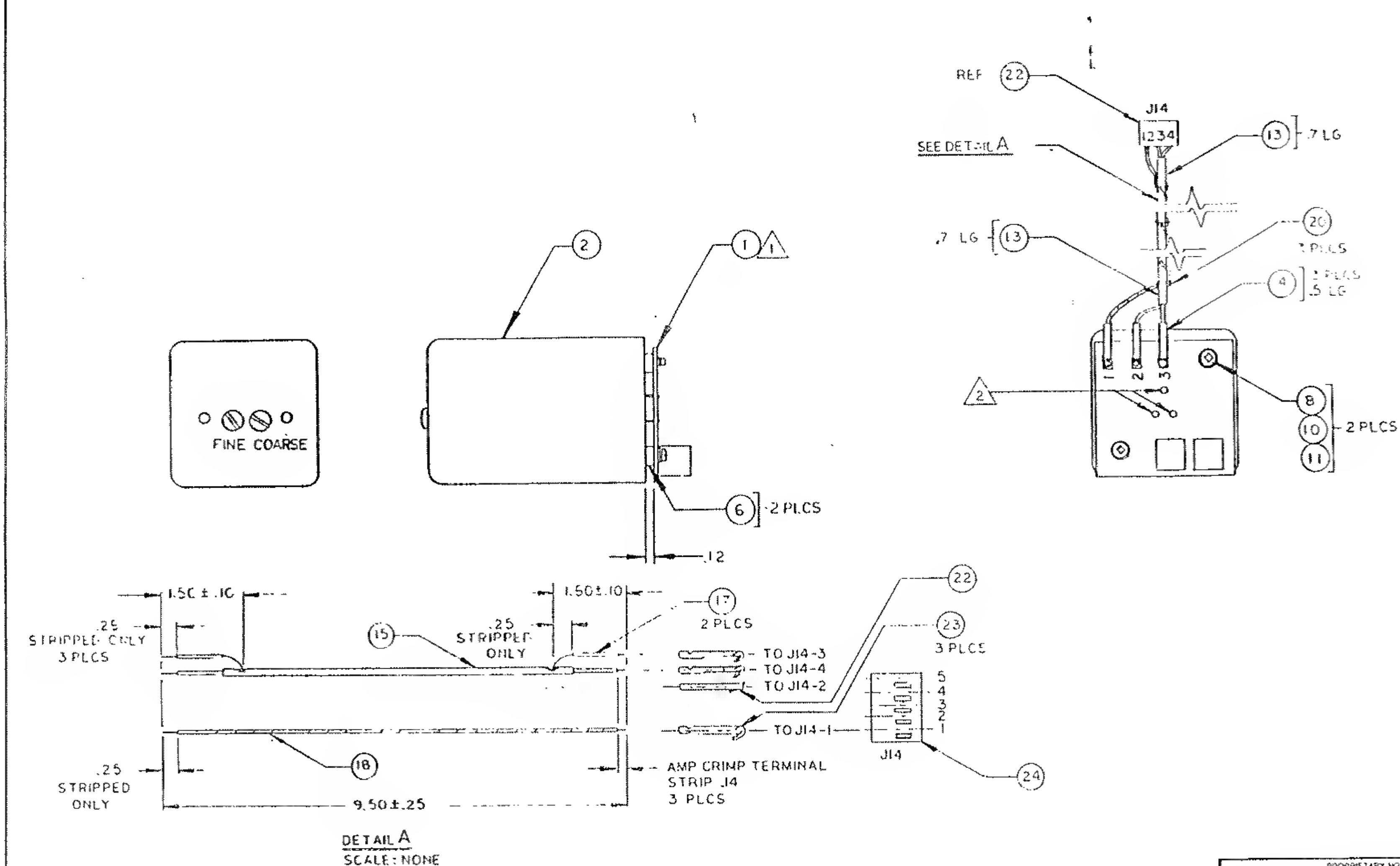


2. REMOVE THE FOLLOWING R/D PART NUMBERS: 10MHZ OSC.PCB ASSY (401730) & SCREW PPH #4-40X.312 & WASHER (616252) 2PLCS.
1. REMOVE CABLE TIE (610777) SECURING CABLES TO J14/P14 AND J13/P13.

RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA 92714

DOCUMENT TITLE
OSC ASSY, OPTION 04E

SIZE	CODE IDENT NO	DOCUMENT NO	REV
C	21793	404384	C



DETAIL A
SCALE: NONE

2. SOLDER AT ASSY.

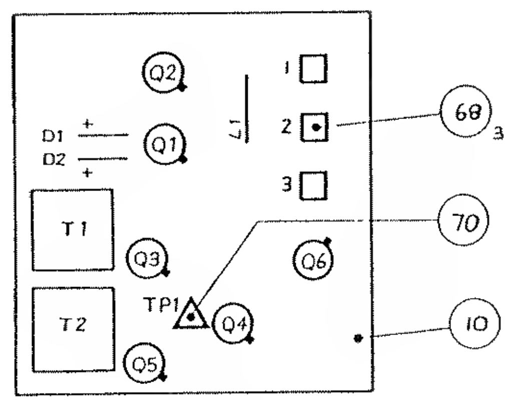
1. REMOVE AND DISCARD CABLE SUPPLIED WITH ITEM 1 AND REPLACE WITH ITEMS: 4,13,15,17,18,20,22,23,24.

NOTES UNLESS OTHERWISE SPECIFIED

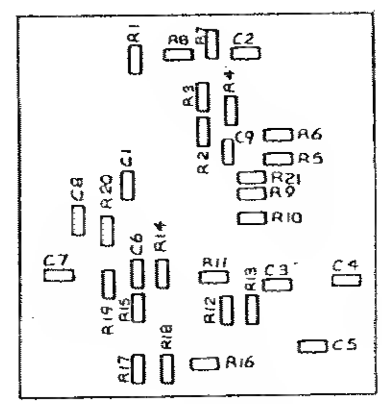
PROPRIETARY NOTICE

RACAL-DANA Instruments Inc.
4 GOODYEAR, IRVINE, CALIFORNIA 92714

DOCUMENT TITLE			
OSCILLATOR ASSY			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
C	21793	404386	C
SCALE —		SHEET 1 OF 3	



VIEWED FROM COMPONENT SIDE

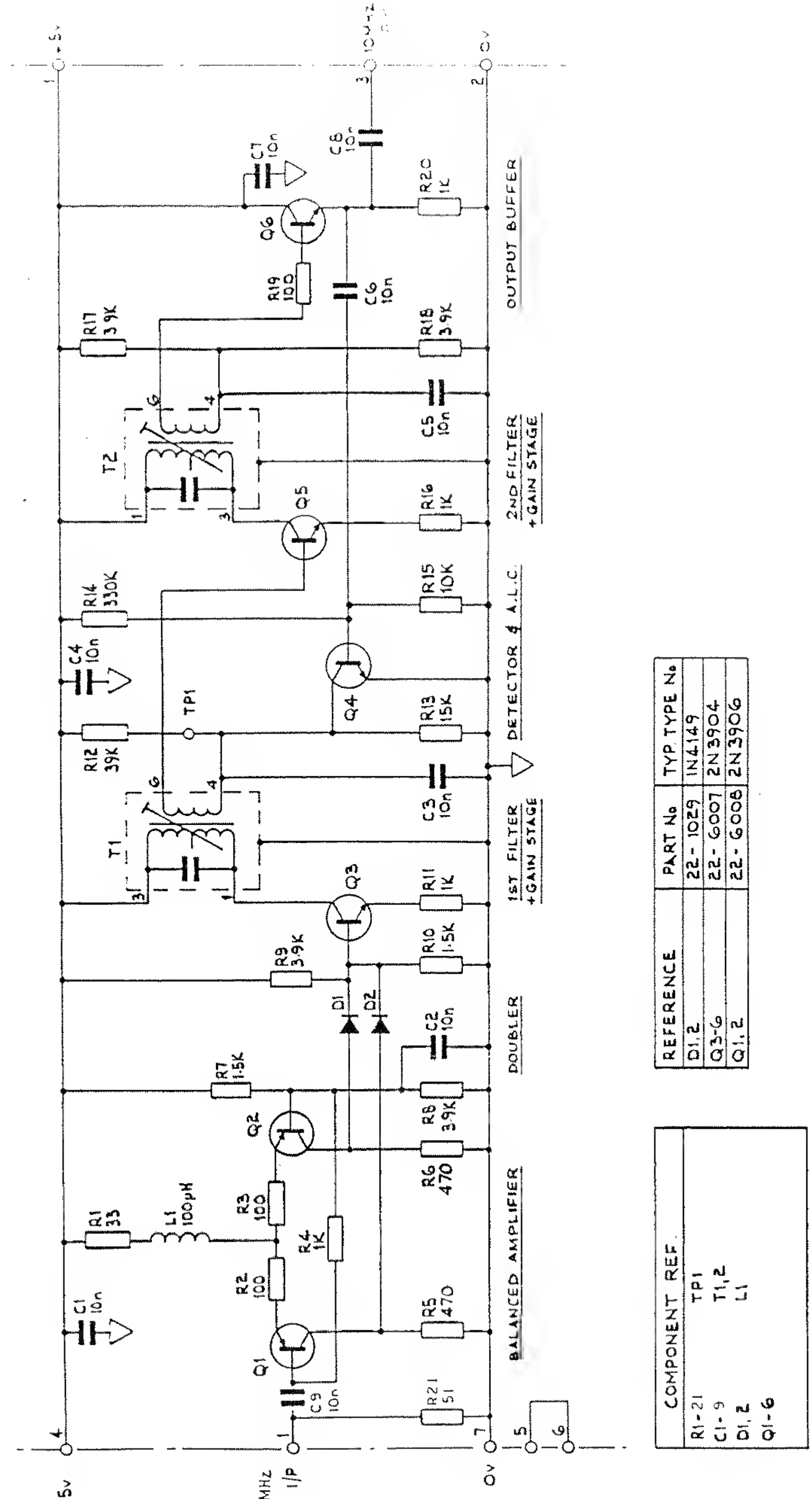


VIEWED FROM TRACK SIDE
(CIRCUIT SIDE)

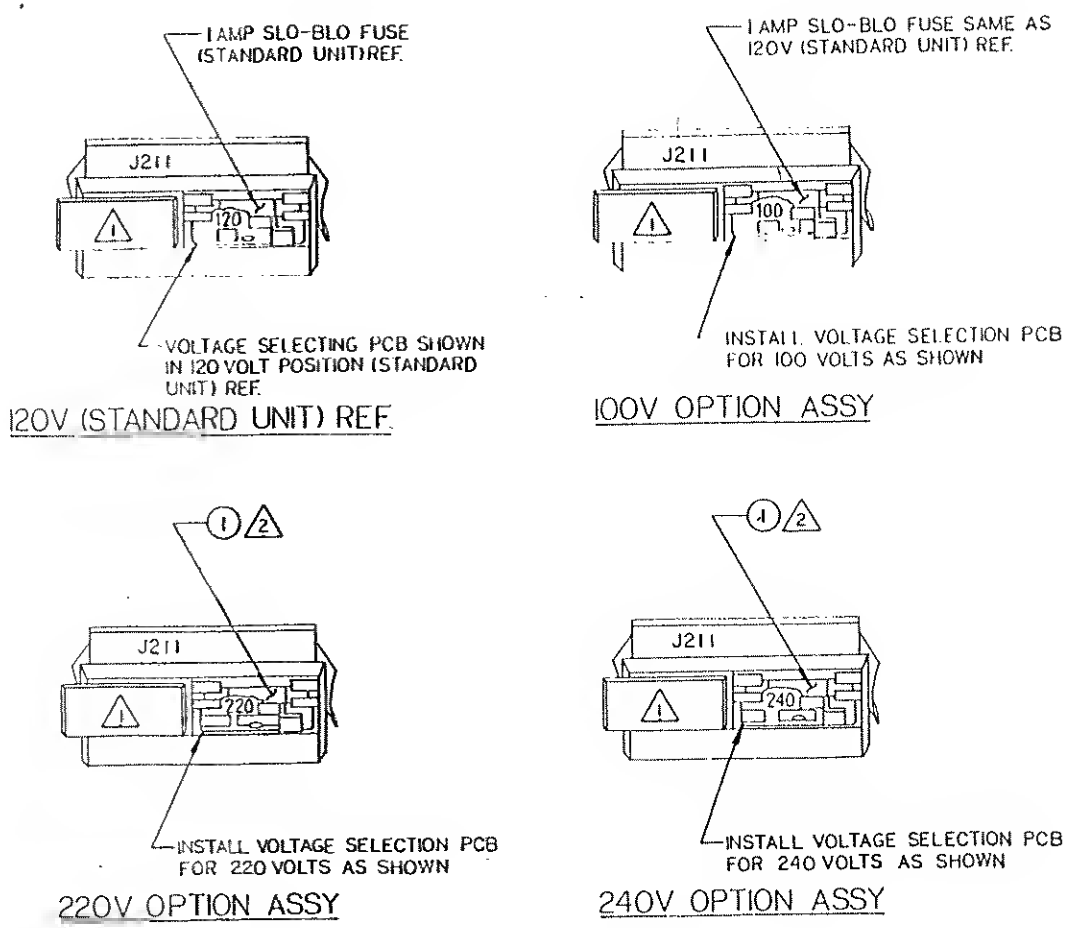
NOTES

1. FIT PIN PART No. 24-3519 ITEM No. 68 IN HOLE POSITIONS MARKED □ TO PROTRUDE ON COMPONENT SIDE. 3OFF

2. FIT PIN PART No. 24-3537 ITEM No 70 IN HOLE POSITIONS MARKED △ TO PROTRUDE ON COMPONENT SIDE 1OFF



Circuit Diagram, Doubler (431822)



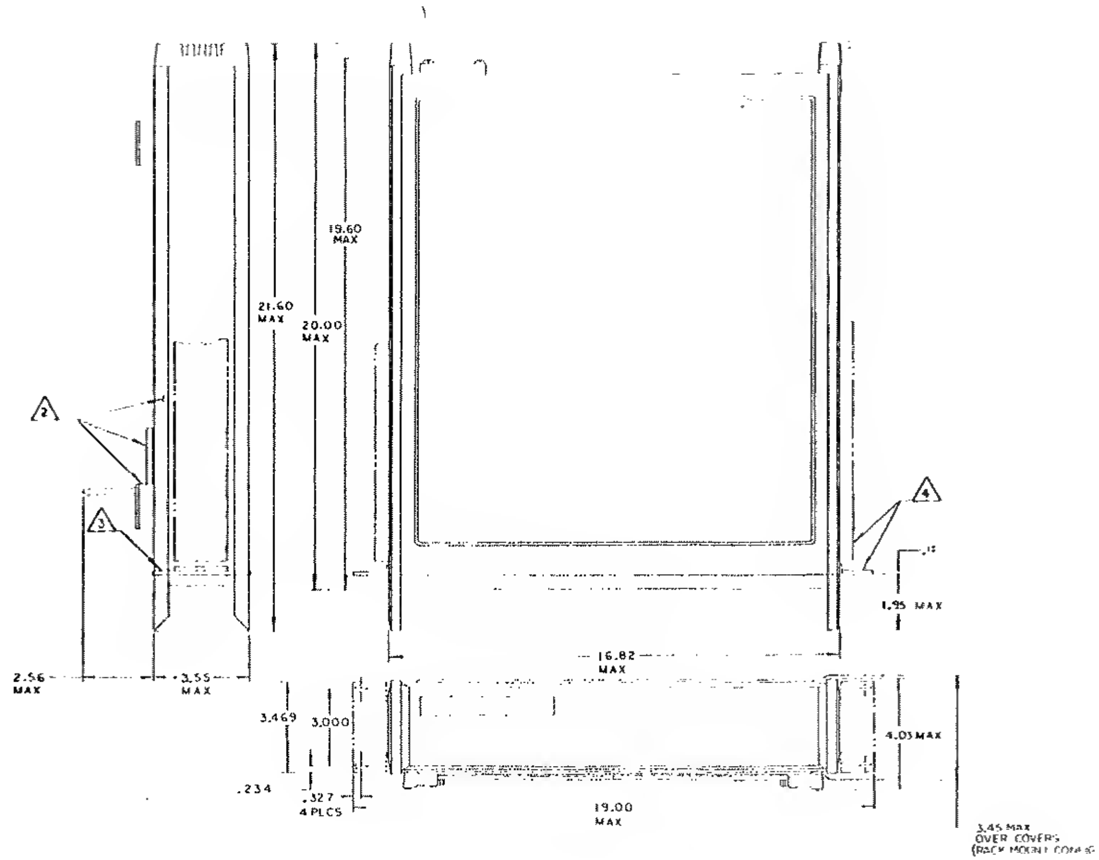
3. SERIAL NUMBER LABEL SHOULD BE MARKED AS REQUIRED TO SUIT SPECIFIC OPTION TO INDICATE CORRECT VOLTAGE.

2. REMOVE AND RETURN STANDARD FUSE TO STOCK.

1. FUSE AND PCB ACCESS COVER SHOWN IN OPEN POSITION.

NOTES UNLESS OTHERWISE SPECIFIED

220V/240V OPERATION, OPTION 71			
SIZE C	CODE IDENT NO. 21793	404387	A



4. REFERENCE SLIDE RACK MOUNTING KIT 404103.

3. REFERENCE: RACK MOUNTING KIT 404180.

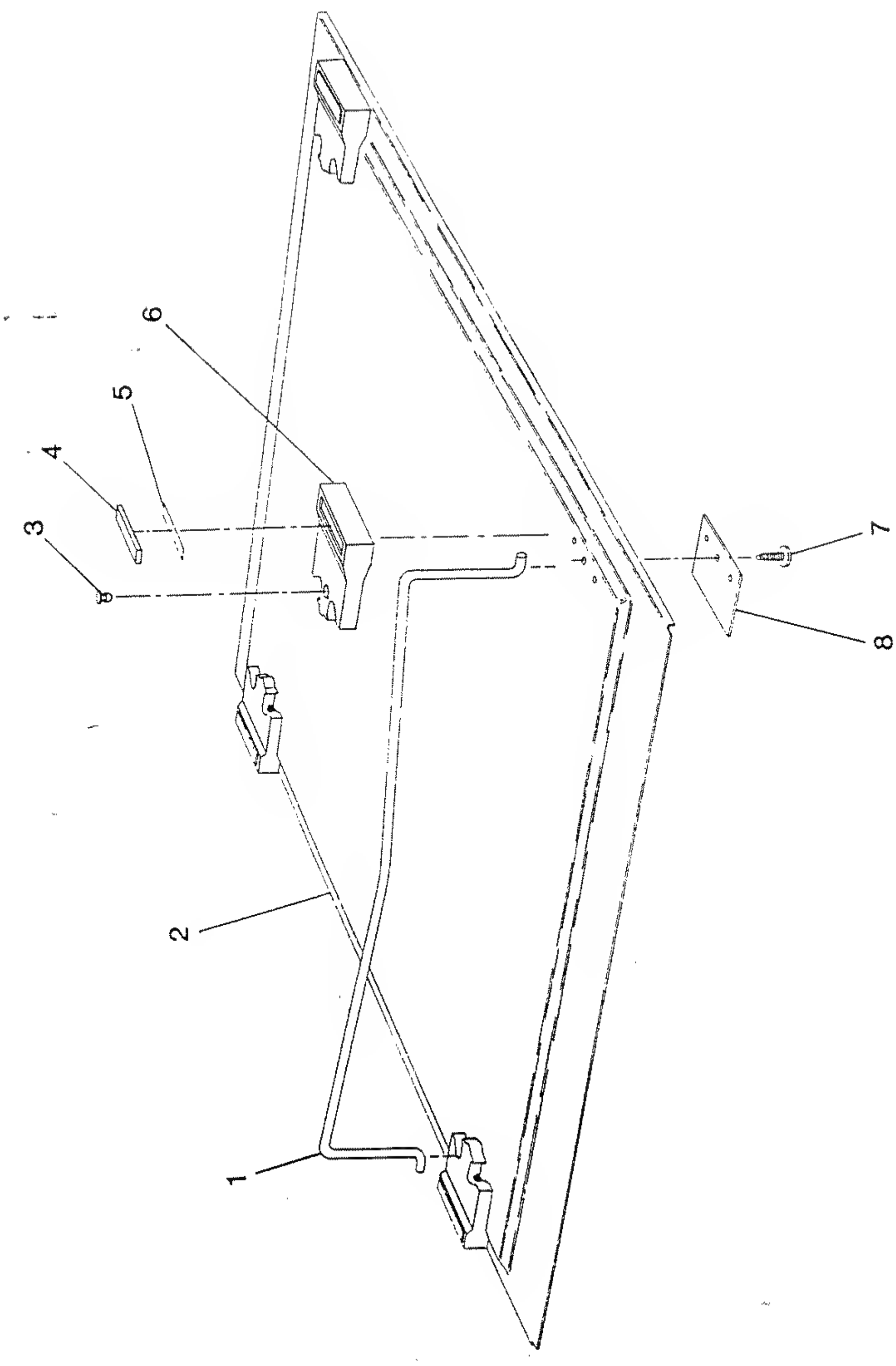
2. FEET, BAIL AND SIDE COVERS ARE REMOVED FOR RACK OR SLIDE INSTALLATION.

1. ALL DIMENSIONS FOR REFERENCE ONLY.

PROPRIETARY NOTICE

OUTLINE DIMENSIONAL SERIES 1990

D	21793	A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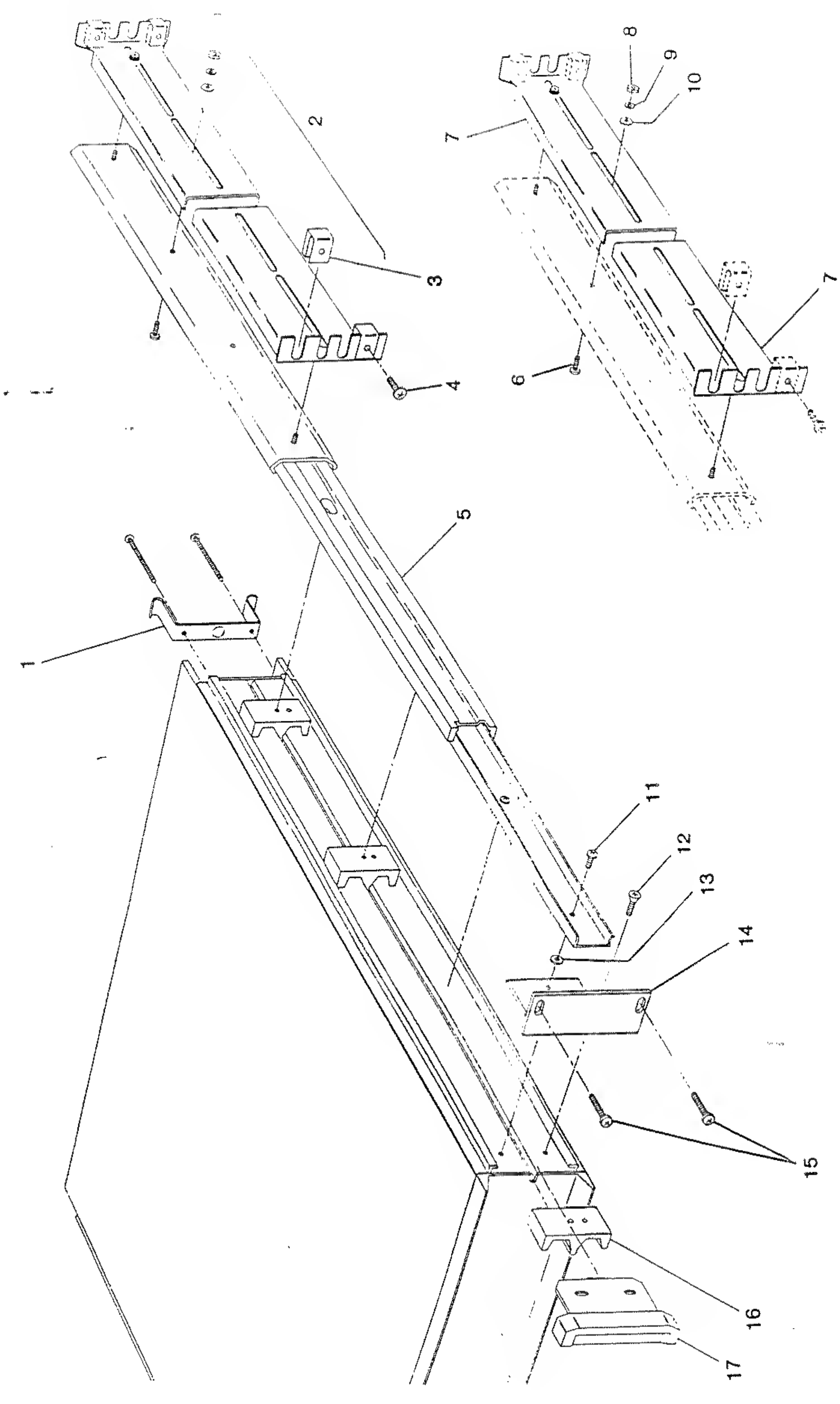
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SECTION 8 PARTS LIST

8.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

8.2 Manufacturers are identified by FSC numbers listed in table 8.1, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

Table 7.1 - List of Suppliers

FSC	Name
00779	Amp, Inc. Harrisburg, PA
00853	Sangamo Electric Co. Pickens, SC
01295	Texas Instruments, Inc. Dallas, TX
02114	Ferroxcube Corp. Saugerties, NY
02735	RCA-Solid State Division Somerville, NJ
04713	Motorola, Inc. Semi-Conductor Division Phoenix, AZ
05245	Corcom, Inc. Chicago, IL
05397	Union Carbide Corp. Material Systems Division Cleveland, OH
05972	Loctite Corp. Hartford, CT
06540	Amatom Electronic Hardware New Rochelle, NY
06776	Robinson Nugent, Inc. New Albany, IN
07263	Fairchild Semi-Conductor Division Mountain View, CA
09023	Cornell-Dubilier Electronics Sanford, NC
11236	CTS of Berne, Inc. Berne, IN
11532	Teledyne Northridge, CA
12969	Unitrode Corp. Watertown, MA
13103	Thermalloy, Inc. Dallas, TX
14433	ITT Semiconductors West Palm Beach, FL
14908	Electronic Instrument & Specialty Corp. Stoneham, MA
14949	Trompeter Electronics Chatsworth, CA
15636	Elec-Trol, Inc. Saugus, CA
17856	Siliconix, Inc. Santa Clara, CA
18324	Signetics Corp. Sunnyvale, CA
18565	Chromerics, Inc. Woburn, MA
19505	Applied Engineering Products New Haven, CT
19647	Caddock Riverside, CA
19738	Avdel-Chobert Teleboro, NJ
1CJ86	Bossard Brookfield, CT
21317	Electronic Applications Co. So. El Monte, CA
21793	Racal-Dana Instruments Inc. Irvine, CA
22119	Ferranti Electric Plainview, NY
24355	Analog Devices Norwood, MA
25088	Siemens Corp. Components Group Iselin, NJ
27014	National Semi-Conductor Corp. Santa Clara, CA
27264	Molex Products Co. Downers Grove, IL
27777	Varo Electran Devices, Inc. Garland, TX
28520	Heyco Kenilworth, NJ
29005	Storm Products Los Angeles, CA
31918	ITT Schadow, Inc. Eden Prarie, MN
32293	Intersil, Inc. Cupertino, CA
32559	Bivar, Inc. Santa Ana, CA
32997	Bourns Trimpot Products Division Riverside, CA
34553	Amperex/Mepco-Electra (Component Division) Hauppauge, NY
34785	Dek-Inc. St. Charles, IL
46384	Penn Engineering & Mfg. Corp. Doylestown, PA
50434	Hewlett-Packard Co. HPA Division Palo Alto, CA
50579	Litronix, Inc. Cupertino, CA
52072	Circuit Assembly Corp. Costa Mesa, CA
52531	Hitachi Magnetics Corp. Edmore, MI
52648	Plessey Memories Santa Ana, CA
53421	Tyton Corp. Milwaukee, WI
54473	Matsushita Electric Co. Secaucus, NJ
55167	Corona Magnetics Corona, CA
55322	Samtec, Inc. New Albany, IN
55411	California Crystal Inc. Anaheim, CA
56235	State of the Art Inc. State College, PA
56289	Sprague Electric Co. Pacific Division Los Angeles, CA
57856	Kel-Am Inc. Eldon, MO
59311	Communication Instruments El Segundo, CA
61394	Seeq Technology San Jose, CA
65940	Rohm Corp. Irvine, CA
70903	Beldon Corp. Chicago, IL
71590	Centralab Electronics Milwaukee, WI

FSC	Name
71707	Coto-Coil Co., Inc. Providence, RI
71785	TRW Electronic Components Cinch Division Elk Grove, IL
72136	Electro motive Mfg. Co., Inc. Willimantic, CT
72982	Erie Technological Products, Inc. Erie, PA
73138	Beckman Instruments, Inc. Fullerton, CA
75915	Littelfuse, Inc. Des Plaines, IL
76493	J. W. Miller Co. Compton, CA
78189	Illinois Tool Works, Inc. Shakeproof Division Elgin, IL
79963	Zierick Mfg. Corp. New Rochelle, NY
80031	Mepco-Electra Morristown, NJ
80131	Electronics Industries Associates Washington, DC

FSC	Name
81349	Military Specification
83125	Nytronics, Inc. Darlington, SC
83330	Herman H. Smith, Inc. Brooklyn, NY
86928	Seastrom Mfg. Co. Glendale, CA
88245	Litton Precision Products Van Nuys, CA
91506	Augut, Inc. Attleboro, MA
91637	Dale Electronics, Inc. Columbus, NE
95275	Vitramon, Inc. Bridgeport, CT
95987	Weckesser Co., Inc. Chicago, IL
98291	Sealectro Corp. Mamaroneck, NY
NOTE 1	RPM Enterprises Santa Ana, CA
NOTE 2	Res-Net Corp. Whippany, NJ
NOTE 3	Universal Components Co. Marquardt Products Los Angeles, CA

404335-COUNTER ASSY., MODEL 1995

B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	404293	COVER ASSY., BOTTOM	21793	404293
2	401730	PCB ASSY., 10 MHZ, OSCILLATOR	21793	401730
3	404332	CHASSIS ASSY	21793	404332
4	454319	FOOT REAR (2 REQ'D)	21793	404319
6	454344	PANEL, SIDE COVER (2 REQ'D)	21793	454344
7	454352	PANEL, TOP COVER	21793	454352
9	454393	HANDLE ASSY (2 REQ'D)	21793	454393
11	454768	BUMPER, REAR FOOT (2 REQ'D)	21793	454768
12	454769	OVERLAY, FRONT PANEL	21793	454769
13	454770	OVERLAY, REAR PANEL	21793	454770
14	610777	CABLE TIE	53421	T18R
15	600620	CABLE, POWER AC LINE	70903	XHS-7041
16	610231	BUTTON PLUG, PLASTIC (4 REQ'D)	28520	P-500
17	610379	WASHER, FLAT, #4, NYLON (4 REQ'D)	95987	AW4-2512
18	616252	SCREW, PPH, SEMS ASSY (2 REQ'D)	21793	616252
19	615073	SCREW, PPH, 8-32 X .312 (4 REQ'D)	—	—
20	610925	SCREW, PPH, 6-32 X 1.00 (4 REQ'D)	78189	—
21	611026	NUT, HEX, 112-28 (6 REQ'D)	00779	1-329631-1
22	611027	WASHER, LOCK, INT, 112 (6 REQ'D)	00779	1-329632-2
23	616255	SCREW, PPH, SEMS ASSY., 6-32 X .312 (7 REQ'D)	78189	—
24	920888	LABEL, IDENTIFICATION	21793	920888
25	980599	MANUAL, INSTRUCTION	21793	980599

404336-COUNTER ASSY., MODEL 1996 Figure 7-3 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	404293	COVER ASSY., BOTTOM	21793	404293
2	401730	PCB ASSY., 10 MHZ, OSCILLATOR	21793	401730
3	404332	CHASSIS ASSY	21793	404332
4	454319	FOOT REAR (2 REQ'D)	21793	404319
6	454344	PANEL, SIDE COVER (2 REQ'D)	21793	454344
7	454352	PANEL, TOP COVER	21793	454352
9	454393	HANDLE ASSY (2 REQ'D)	21793	454393
11	454768	BUMPER, REAR FOOT (2 REQ'D)	21793	454768
12	454769	OVERLAY, FRONT PANEL	21793	454769
13	454770	OVERLAY, REAR PANEL	21793	454770
14	610777	CABLE TIE	53421	T18R
15	600620	CABLE, POWER AC LINE	70903	KHS-7041
16	610231	BUTTON PLUG, PLASTIC (4 REQ'D)	28520	P-500
17	610379	WASHER, FLAT, #4, NYLON (4 REQ'D)	95987	NW4-2812
18	616252	SCREW, PPH, SEMS ASSY (2 REQ'D)	21793	616252
19	615073	SCREW, PPH, 8-32 X .312 (4 REQ'D)	—	—
20	610925	SCREW, PPH, 6-32 X 1.00 (4 REQ'D)	78189	—
21	611026	NUT, HEX, 112-28 (6 REQ'D)	00779	1-329631-2
22	611027	WASHER, LOCK, INT, 112 (6 REQ'D)	00779	1-329632-2
23	616255	SCREW, PPH, SEMS ASSY., 6-32 X .312 (7 REQ'D)	78189	—
24	920888	LABEL, IDENTIFICATION	21793	920888
25	980599	MANUAL, INSTRUCTION	21793	980599
26	404389	PCB ASSY., CHANNEL C	21793	404389
27	404385	CABLE ASSY., 2 COND.	21793	404385

404336-COUNTER ASSY., MODEL 1996 (CONT'D) Figure 7-3 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG., P/N
28	454868	BRACKET, SUPPORT, CH. C (2 REQ'D)	21793	454868
30	601235	CONNECTOR, BNC, PNL, MTG (J103)	21793	601235
32	610127	WASHER, SHOULDER, #4, NYLON (2 REQ'D)	86928	5607-10
33	610198	WASHER, FLAT, #4, NYLON (2 REQ'D)	86928	5610-10-31
35	611066	SCREW, METRIC, M3X6 (2 REQ'D)	—	—
38	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	—	—

Figure 7-4 D

404332 - ASSY., CHASSIS

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	401725	PCB ASSY., MOTHERBOARD	21793	401725
2	401726	PCB ASSY., SIGNAL COND.	21793	401726
3	401727	PCB ASSY., DISPLAY KEYBOARD	21793	401727
9	192552	FASTENER, LOCK, 14-PIN DIP (2 REQ'D)	52072	CA-14-200-DL
5	404330	ASSY., TRANSFORMER	21793	404330
6	404331	ASSY., REAR PANEL	21793	404331
8	454372	PUSH ROD	21793	454372
10	454390	BLOCK MOUNTING (8 REQ'D)	21793	454390
12	454763	PANEL, FRONT	21793	454763
13	454764	PANEL, SIDE, RIGHT	21793	454764
14	454763	PLATE, SUPPORT, BOTTOM	21793	454736
18	454818	PANEL, SIDE, LEFT	21793	454818
19	454819	SHIELD, SIG. COND., BTM	21793	454819
21	500213-011	TUBING, TYGON, 1.0 LG	21793	500231-011
23	404385	CABLE ASSY., 2 COND.	21793	404385
24	601225	CABLE ASSY., 14, TWIST PR	52072	CA-D14P02-284-IT-010
26	610909	SCREW, PPH, TAPTITE, 6-32 X .500 (6 REQ'D)	78189	—
30	611075	CLAMP, CLUTCH-TYPE	78553	C40588-020-1
37	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (11 REQ'D)	78189	—
38	616255	SCREW, PPH, SEMS ASSY., 6-32 X .312 (9 REQ'D)	78189	—
40	616259	SCREW, PPH, SEMS ASSY., 8-32 X .312 (4 REQ'D)	78189	—
44	921006	BUTTON, PUSH, PWR, RED	21793	921006

401730 - PCB ASSY., 10 MHZ OSCILLATOR A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
P14	611056	CONNECTOR, CABLE, 5 PIN	00779	530554-4
Y1	921013	OSCILLATOR, 10 MHZ	21793	921013
1	411730	PCB, 10 MHZ OSCILLATOR (UNLOADED)	21793	411730
4	524211	WIRE, TEFLON, STRANDED, 24 GA, BRN/RED	—	—
5	524333	WIRE, TEFLON, STRANDED, 24 GA, ORG	—	—
6	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	—	—
8	610160	STANDOFF, 4-40, THRU SWAGE (2 REQ'D)	83330	4103
10	610777	CABLE TIE	53421	181R
12	611052	KEY, POLARIZING, PLUG	00779	87077-1
13	611053	TERMINAL, CRIMP (4 REQ'D)	00779	530553-2

404389, CHANNEL "C" ASSY., 1.3 GHZ

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C2	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C3	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C4	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C5	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C6	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C7	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C8	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C9	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C10	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C11	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C12	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C13	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C14	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C15	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C16	R-21-0795	CAP, ALUM. ELEC., 47 UF, 25V WKG, -10 +50%	54473	ECEA1HK2R2E
C17	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C18	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C19	R-21-1783	CAP, CHIP, 4.7 PF, 50V, ±.25 PF	95275	VJ1206A4R7CXA
C21	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C22	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C23	R-21-1799	CAP, CHIP, 12 PF, 50V, 5%	95275	VJ1206A391JXA
C24	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C25	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C26	R-21-1800	CAP, CHIP, 1 NF, 50V, 20%	95275	VJ1206Y102MXA
C27	R-21-0795	CAP, ALUM. ELEC., 47 UF	54473	ECEA1HK2R2E
C28	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C29	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C30	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C31	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C32	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C33	R-21-1784	CAP, CHIP, 5.6 PF, 50V, ±.25 PF	95275	VJ1206A5R6CXA
C34	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C35	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C36	R-21-1785	CAP, CHIP, 6.8 PF, 50V, ±.25 PF	95275	VJ1206A6R8CXA
C37	R-20-1795	CAP, CHIP, 47 PF, 50V, 5%	95275	VJ1206A470JXA
C38	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C39	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C40	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C41	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C42	R-21-1784	CAP, CHIP, 5.6 PF, 50V, ±.25 PF	95275	VJ1206A5R6CXA
C43	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C44	R-21-0795	CAP, ALUM. ELEC., 47 UF	54473	ECEA1HK2R2E
C45	R-21-0704	CAP, ALUM. ELEC., 47 UF	18324	122-53479
C46	R-21-1782	CAP, CHIP, 3.9 PF, 50V, ±.25 PF	95275	VJ1206A3R9CXA
C47	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA
C48	R-21-1801	CAP, CHIP, 10 NF, 50V, 20%	95275	VJ1206Y103MXA

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C49	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C50	R-21-1781	CAP, CHIP, 3.3 PF, 50V, ±.25 PF	95275	VJ1206A3R3CXA
C51	R-21-1789	CAP, CHIP, 15 PF, 50V, 5%	95275	VJ1206A150JXA
C52	R-21-1789	CAP, CHIP, 15 PF, 50V, 5%	95275	VJ1206A150JXA
C53	100133	CAP, CERAM, .1 UF, 20%, LP	72982	8131LP-100-651-104M
D1	210089	DIODE, SILICO	50434	5082-2835
D2	R-22-1058	DIODE, SILICO	50434	5082-3379
D3	210089	DIODE, SILICO	50434	5082-2835
D5	210089	DIODE, SILICO	50434	5082-2835
D6	210089	DIODE, SILICO	50434	5082-2835
D7	R-22-1058	DIODE, SILICO	50434	5082-3379
D8	210017	DIODE, HOT CARRIER, MATCHED PAIR	21793	210017
D9	210017	DIODE, HOT CARRIER, MATCHED PAIR	21793	210017
D10	R-22-1814	DIODE, ZENER	22119	BZX79C9V1
D11	R-22-1814	DIODE, ZENER	22119	BZX79C9V1
D12	R-22-1029	DIODE, SILICO	14433	1N4149
IC1	230547	IC, QUAD COMPARATOR	27014	LM339N
IC2	230787	IC, TRIPLE LINE RECEIVER	04713	MC10116P
IC3	R-22-4694	IC, 1.3 GHz PRESCALER PLESSEY	52648	SP4730
IC4	230193	IC, TTL LOW POWER SHOTTY NAND GATES	01295	74LS00
L1	R-17-3240	COIL ASSY	21793	R-17-3240

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Q1	R-22-6123	TRANSISTOR	34553	BFR90
Q2	R-22-6123	TRANSISTOR	34553	BFR90
Q3	R-22-6123	TRANSISTOR	34553	BFR90
Q4	R-22-6155	TRANSISTOR	50434	HXTR3101
R3	R-20-5768	RES, CHIP, 10K, 1/8W, 5%	65940	MCR18-10K-5PCT
R4	R-20-5768	RES, CHIP, 10K, 1/8W, 5%	65940	MCR18-10K-5PCT
R5	R-20-5841	RES, CHIP, 150 OHM, 1W	56235	2021CPX151J
R6	R-20-5837	RES, CHIP, 39 OHM, 1W	56235	2021CPX390J
R7	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R8	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%, 200V	65940	MCR18-150-5PCT
R9	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R10	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	65940	MCR18-100-5PCT
R11	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R12	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R13	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R14	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R15	R-20-5786	RES, CHIP, 270 OHM, 1/8W, 5%, 200V	65940	MCR18-270-5PCT
R16	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	65940	MCR18-390-5PCT
R18	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R19	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R20	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R21	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5%, 200V	65940	MCR18-180-5PCT
R22	R-20-5784	RES, CHIP, 180 OHM, 1/8W, 5%, 200V	65940	MCR18-180-5PCT
R23	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	65940	MCR18-390-5PCT
R24	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT

404389, CHANNEL "C" ASSY., 1.3 GHZ (CONT'D)

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R25	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33-5PCT
R26	R-20-5787	RES, CHIP, 330 OHM, 1/8W, 5%, 200V	65940	MCR18-330-5PCT
R27	R-20-7049	POT, 20K	73138	72XLR20K
R28	R-20-5788	RES, CHIP, 390 OHM, 1/8W, 5%, 200V	06540	MCR18-390-5PCT
R29	R-20-5813	RES, CHIP, 100K, 1/8W, 5%, 200V	06540	MCR18-100K-5PCT
R30	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	06540	MCR18-10-5PCT
R31	R-20-5774	RES, CHIP, 22 OHM, 1/8W, 5%, 200V	06540	MCR18-22-5PCT
R32	R-20-5785	RES, CHIP, 220 OHM, 1/8W, 5%, 200V	06540	MCR18-220-5PCT
R33	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	06540	MCR18-1.5K-5PCT
R34	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	06540	MCR18-1.5K-5PCT
R35	R-20-5810	RES, CHIP, 56K, 1/8W, 5%, 200V	06540	MCR18-56K-5PCT
R36	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	06540	MCR18-10-5PCT
R37	R-20-5779	RES, CHIP, 56 OHM, 1/8W, 5%, 200V	06540	MCR18-56-5PCT
R38	R-20-5810	RES, CHIP, 56K, 1/8W, 5%, 200V	06540	MCR18-56K-5PCT
R39	R-20-5770	RES, CHIP, 1M, 1/8W, 5%, 200V	06540	MCR18-1M-5PCT
R41	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5%, 200V	06540	MCR18-4.7K-5PCT
R42	R-20-5799	RES, CHIP, 4.7K, 1/8W, 5%, 200V	06540	MCR18-4.7K-5PCT
R44	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	06540	MCR18-1K-5PCT
R45	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%, 200V	06540	MCR18-150-5PCT
R46	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R47	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R48	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R49	R-20-5775	RES, CHIP, 27 OHM, 1/8W, 5%, 200V	06540	MCR18-27-5PCT
R50	R-20-5765	RES, CHIP, 470 OHM, 1/8W, 5%, 200V	06540	MCR18-470-5PCT

404389, CHANNEL "C" ASSY. 1.3 GHZ (CONT'D)

Figure 7-8

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R52	R-20-5801	RES, CHIP, 6.8K, 1/8W, 5%, 200V	06540	MCR18-6.8K-5PCT
R53	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5%, 200V	06540	MCR18-3.3K-5PCT
R54	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	06540	MCR18-1K-5PCT
R55	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R56	R-20-5790	RES, CHIP, 680 OHM, 1/8W, 5%, 200V	65940	MCR18-680-5PCT
R57	R-20-5766	RES, CHIP, 2.7K, 1/8W, 5%	65940	MCR18-2.7K-5PCT
R58	R-20-5797	RES, CHIP, 3.3K, 1/8W, 5%, 200V	65940	MCR18-3.3K-5PCT
R59	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R60	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R61	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R62	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5PCT
R66	R-20-5783	RES, CHIP, 150 OHM, 1/8W, 5%	65940	MCR18-150-5PCT
R68	R-20-5770	RES, CHIP, 1M, 1/8W, 5%	65940	MCR18-1M-5PCT
R69	R-20-5770	RES, CHIP, 1M, 1/8W, 5%	65940	MCR18-1M-5PCT
R70	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
R71	R-20-5771	RES, CHIP, 10 OHM, 1/8W, 5%, 200V	65940	MCR18-10-5PCT
SK7	R-23-5173	CONNECTOR, 30 WAY	21793	R-23-5173
3	601257	CABLE ASSEMBLY	19505	80-1151-1425
4	601256	CONNECTOR	19505	2009-7511-000
6	R-13-2103	SCREEN (2 REQ'D)	21793	R-13-2103
7	R-13-2104	COVER (2 REQ'D)	21793	R-13-2104
8	R-14-4000	SPACER (2 REQ'D)	21793	R-14-4000
10	R-18-1142	P.C. BOARD (UNLOADED)	21793	R-18-1142
156	617042	NUT, HEX, M3 (2 REQ'D)	1CJ86	01N934-ME
158	R-24-2801	WASHER, CRINKLE, M3 (2 REQ'D)	21793	R-24-2801
166	500022	WIRE, BARE COPPER/TIN, 22GA	21793	500022

401725 - PCB ASSY., MOTHERBOARD

Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C2	110215	CAP, TANTA, 1.5 MFD, 25V, 10%	80031	41GS155A025K1A
C3	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C4	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-103K
C5	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C6	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C7	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C8	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-103K
C9	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-103K
C10	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-103K
C11	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-103K
C12	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C13	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5R0-013K
C14	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C15	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C16	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C17	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C18	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C19	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D)

Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C20	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C21	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C22	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C23	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C24	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C25	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C26	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C27	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C28	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C29	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C30	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C31	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C32	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C33	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C34	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C35	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C36	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C37	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C38	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C39	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C40	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C41	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C42	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C43	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C44	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C45	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C46	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C47	100062	CAP, CERAM. .01 MFD, 100V. 10%	72982	8121-100-W5R0-103K
C48	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C49	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C50	100062	CAP, CERAM, .01 MFD, 100V. 10%	72982	8121-100-W5R0-103K
C51	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C52	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C53	110151	CAP, TANTA, 10 MFD, 35V. 20%	05397	T354G106M035AS

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C54	100062	CAP, CERAM, .01 MFD, 100V. 10%	72982	8121-100-W5R0-103K
C55	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C56	110151	CAP, TANTA. 10 MFD, 35V. 20%	05397	T354G106M035[illegible]
C57	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035[illegible]
C58	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C59	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C60	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C61	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C62	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035[illegible]
C63	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C64	100062	CAP. CERAM. .01 MFD. 100V. 10%	72982	8121-100-W5R0-103K
C65	110126	CAP, TANTA, 6.8 MFD. 35V, 20%	05397	T355F685M035[illegible]
C66	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C67	100133	CAP, CERAM, .1 MFD. LOW PROFILE. 20%	72982	8131LP-100-651-104M
C68	110126	CAP, TANTA. 6.8 MFD. 35V, 20%	05397	T355F685M035[illegible]
C69	100062	CAP, CERAM, .01 MFD. 100V. 10%	72982	8121-100-W5R0-103K
C70	100062	CAP, CERAM, .01 MFD. 100V. 10%	72982	8121-100-W5R0-103K
C71	100062	CAP, CERAM. .01 MFD. 100V. 10%	72982	8121-100-W5R0-103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C72	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5RO-103K
C73	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5RO-103K
C74	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5RO-103K
C75	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5RO-103K
C76	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100W5RO-103K
C77	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C78	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C79	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C80	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C81	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C82	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C83	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C84	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C85	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C86	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C87	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C88	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C89	110218	CAP, TANTA, 47 MFD, 20V, 20%	56289	199047 [illegible] EE2
C90	110218	CAP, TANTA, 47 MFD, 20V, 20%	56289	199047 [illegible] EE2
C91	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible]-103K
C92	110217	CAP, AE, 1000 MFD, 35V, RADIAL	80031	3475 [illegible] M8S
C93	110217	CAP, AE, 1000 MFD, 35V, RADIAL	80031	3475 [illegible] M8S
C94	110214	CAP, AE, 10000 MFD, 16V	00853	380-103-[illegible]-J04
C95	110214	CAP, AE, 10000 MFD, 16V	00853	380-103-[illegible]-J04
C96	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	[illegible]
C97	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible]-103K
C98	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible]-103K
C99	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035[illegible]
C100	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible]-103K
C101	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C102	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible]-103K
C103	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C104	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035[illegible]
C105	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R[illegible]-103K

401725 - PCB ASSY,, MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C106	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C107	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C108	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C109	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C110	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C111	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C112	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C113	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C114	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C115	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C116	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C117	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C118	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C119	110219	CAP, AE, 3300 MFD, 16V, 20%	80031	3476KL332M016
C120	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C121	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C122	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C123	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K

401725 - PCB ASSY,, MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C124	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C125	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C126	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C127	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C128	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035
C129	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C130	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C131	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C132	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C133	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C134	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C135	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C136	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C137	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C138	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K
C139	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R 103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C140	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C141	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C142	130171	CAP, TRIMMER, CERAM, 5-25 PFD, 250V	56289	GKU25000
C143	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C144	100065	CAP, CERAM, .0022 MFD, 1000V, 10%	71590	DD222
C145	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C146	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C147	100062	CAP, CERAM, .01 MFD. 100V, 10%	72982	8121-100-W5R0-103K
C148	100062	CAP, CERAM, .01 MFD. 100V. 10%	72982	8121-100-W5R0-103K
C149	130094	CAP, MICA, 220 PFD, 500V. 5%	72136	SCDM10-221J
C150	130094	CAP, MICA, 220 PFD, 500V, 5%	72136	SCDM10-221J
C151	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C152	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C153	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C154	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C155	100106	CAP, CERAM, 100 PFD, 1000V, 10%	56289	10-TS-T10
C156	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C157	100062	CAP, CERAM, .01 MFD, 100V. 10%	72982	8121-100-W5R[illegible] 103K
C158	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035-[illegible]
C159	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R[illegible] 103K
C160	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5[illegible] 103K
C161	100062	CAP, CERAM, .01 MFD. 100V, 10%	72982	8121-100-[illegible] 103[illegible]
C162	100116	CAP, CERAM, 500 PFD, 100[illegible]V. 20%	56289	C023B10[illegible]
C163	100142	CAP, CERAM, 82 PFD, 100V, 5%	05397	C320C820[illegible]
C164	100071	CAP, CERAM, .001 MFD, 1000V. 20%	56289	C023B10[illegible]
C165	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354[illegible]
C166	100062	CAP, CERAM, .01 MFD. 100V. 10%	72982	[illegible]
C167	100062	CAP, CERAM, .01 MFD, 100V. 10%	72982	8121-100-[illegible] 103K
C168	110151	CAP, TANTA, 10 MFD. 35V. 20%	05397	T354G10[illegible]
C169	100062	CAP, CERAM. .01 MFD. 100V, 10%	72982	8121-100-W5R[illegible] 103K
C170	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5[illegible] 103K
C171	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5[illegible] 103K
C172	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R[illegible] 103K
C173	100116	CAP, CERAM, 500 PFD. 1000V. 20%	56289	C023B102[illegible]M
C174	100062	CAP, CERAM. .01 MFD. 100V. 10%	72982	8121-100-W5R[illegible] 103K

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C175	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C176	100124	CAP, CERAM, 330 PFD, 1KV, 20%	56289	C023B102E331M
C177	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C178	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C179	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C180	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C181	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
CR1	230551	IC, VOLTAGE REFERENCE	24355	AD589JH
CR2	211083	DIODE, SILICO	81349	1N916B
CR3	220095	DIODE, ZENER, DUAL, 18V	SEE NOTE 1 TABLE 7.1	DM503CC100SP
CR4	220100	DIODE ARRAY, 11 ZENERS, SIP, 6.2V	SEE NOTE 1 TABLE 7.1	DM512CC100SP
CR5	210004	DIODE, SILICO	81349	1N4004
CR6	210004	DIODE, SILICO	81349	1N4004
CR7	211083	DIODE, SILICO	81349	1N916B
CR8	230594	IC, FULL WAVE RECT. BRIDGE	27777	VH148
CR9	210004	DIODE, SILICO	81349	1N4004
CR10	210004	DIODE, SILICO	81349	1N4004
CR11	210004	DIODE, SILICO	81349	1N4004
CR12	211083	DIODE, SILICO	81349	1N916B
CR13	211083	DIODE, SILICO	81349	1N916B

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
CR14	211083	DIODE, SILICO	81349	1N916B
CR15	211083	DIODE, SILICO	81349	1N916B
CR16	211083	DIODE, SILICO	81349	1N916B
CR17	211083	DIODE, SILICO	81349	1N916B
CR18	211083	DIODE, SILICO	81349	1N916B
CR19	211083	DIODE, SILICO	81349	1N916B
CR20	210004	DIODE, SILICO	81349	1N4004
CR21	210102	DIODE, VARACTOR, SILICO	04713	MV1632
CR22	220099	DIODE, ZENER, 4,7V	04713	1N5993B
CR23	211083	DIODE, SILICO	81349	1N916B
CR24	220012	DIODE, SILICO, ZENER	81349	1N958B
CR25	220012	DIODE, SILICO, ZENER	81349	1N958B
CR26	220101	DIODE, ZENER, 3.3V, 5%	04713	[illegible]
F1	920930	FUSE, NORMAL BLO, 6A, 250V	75915	312006
F2	920930	FUSE, NORMAL BLO, 6A, 250V	75915	312006
J1	601192	CONNECTOR, PCB, 34P	52072	CA-034-230-4[illegible]
J2	600798	CONNECTOR, PLUG, 3P	27264	09-18-503[illegible]
J4	601221	CONNECTOR, EDGE, RECEPT., 20P	71785	50-20SN-4
J9	601214	CONNECTOR, EDGE, RECEPT., 72P	57886	RCR36-614-[illegible]
J10	601221	CONNECTOR, EDGE, RECEPT., 20P	71785	50-20SN-4
J11	601217	CONNECTOR, PWR, PLUG, 15P	00779	9-350267-[illegible]
J12	601217	CONNECTOR, PWR, PLUG, 15P	00779	9-350267-[illegible]
J13	601218	CONNECTOR, PWR, PLUG, 6P	00779	9-350255-[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
J14	601208-012	CONNECTOR, PCB, PLUG, 5P	21793	601208-012
J15	601208-013	CONNECTOR, PCB, PLUG, 30P	21793	601208-013
J16	600947	SOCKET, IC, 20P	52072	CA-20S-TSD-BC
J17	920734	SOCKET, IC, 14P	00779	583527-1
J18	601208-010	CONNECTOR, PCB, PLUG, 2P	21793	601208-010
J19	601208-010	CONNECTOR, PCB, PLUG, 2P	21793	601208-010
J20	601208-011	CONNECTOR, PCB, PLUG, 4P	21793	601208-011
J21	600947	SOCKET, IC, 20P	52072	CA-20S-TSD-BC
J203	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
J204	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
J205	601253	CONNECTOR, GPIB, 24P	00779	553811-3
J206	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
J207	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
J208	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
J209	601231	CONNECTOR, BNC, PC MOUNT	00779	227161-2
L1	310051	CHOKE, RF, 1.00 VH, 10%	76493	9230-20
L2	310051	CHOKE, RF, 1.00 VH, 10%	76493	9230-20
L3	310051	CHOKE, RF, 1.00 VH, 10%	76493	9230-20
Q1	200295	TRANS, N-CHAN, MOS FET	17856	VN10KM
Q2	200299	TRANS, PNP	04713	2N3906
Q3	200298	TRANS, NPN	04713	2N3904

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Q4	200068	TRANS, PNP	80131	2N4250
Q5	200068	TRANS, PNP	80131	2N4250
Q6	200298	TRANS, NPN	04713	2N3904
Q7	200252	TRANS, J-FET	27014	J174
Q8	200296	TRANS, P-CHAN, J-FET	17856	J177
Q9	200298	TRANS, NPN	04713	2N3904
Q10	200278	TRANS, PWR, SCR	04713	2N6504
Q11	200278	TRANS, PWR, SCR	04713	2N6504
Q12	200258	TRANS	07263	2N4248
Q13	200258	TRANS	07263	2N4248
Q14	200298	TRANS, NPN	04713	2N3904
Q15	200298	TRANS, NPN	04713	2N3904
Q16	200068	TRANS, PNP	80131	2N4250
R1	000104	RES, CARBON, 100K, 5%, 1/4W	81349	RC07GF104J
R2	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R3	000112	RES, CARBON, 1.1K, 5%, 1/4W	81349	[illegible]
R4	000104	RES, CARBON, 100K, 5%, 1/4W	81349	[illegible]
R5	000105	RES, CARBON, 1M, 5%, 1/4W	81349	[illegible]
R6	000474	RES, CARBON, 470K, 5%, 1/4W	81349	[illegible]
R7	000225	RES, CARBON, 2.2M, 5%, 1/4W	81349	[illegible]
R8	012004	RES, METAL, 4.12K, 1%, 1/8W	81349	[illegible]
R9	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	[illegible]
R10	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	[illegible]
R11	010392	RES, METAL, 20K, .1%, 1/8W	81349	[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R12	000512	RES, CARBON, 5.1K, 5%, 1/4W	81349	RC07GF512J
R13	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R14	010392	RES, METAL, 20K, 1%, 1/8W	81349	RN55C2002B
R15	000512	RES, CARBON, 5.1K, 5%, 1/4W	81349	RC07GF512J
R16	010086	RES, METAL, 9.53K, 1%, 1/4W	81349	RN60D9531F
R17	010385	RES, METAL, 19.1K, 1%, 1/4W	81349	RN60D1912F
R18	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	RC07GF221J
R19	010086	RES, METAL, 9.53K, 1%, 1/4W	81349	RN60D9531F
R20	010385	RES, METAL, 19.1K, 1%, 1/4W	81349	RN60D1912F
R21	000222	RES, CARBON, 2.2K, 5%, 1/4W	81349	RC07GF222J
R22	000622	RES, CARBON, 6.2K, 5%, 1/4W	81349	RC07GF622J
R23	000331	RES, CARBON, 330 OHM, 5%, 1/4W	81349	RC07GF331J
R24	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	RC07GF472J
R25	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R26	000470	RES, CARBON, 47 OHM, 5%, 1/4W	81349	RC07GF470J
R27	000331	RES, CARBON, 330 OHM, 5%, 1/4W	81349	RC07GF331J
R28	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R29	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R30	000432	RES, CARBON, 4.3K, 5%, 1/4W	81349	RC07GF432J
R31	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R32	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	RC07GF472J
R33	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	RC07GF472J
R34	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	RC07GF472J
R35	000104	RES, CARBON, 100K, 5%, 1/4W	81349	RC07GF104J

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R36	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	[illegible]
R37	000102	RES, CARBON, 1K, 5%, 1/4W	81349	[illegible]
R38	000333	RES, CARBON, 33K, 5%, 1/4W	81349	[illegible]
R39	000470	RES, CARBON, 47 OHM, 5%, 1/4W	81349	[illegible]
R40	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	[illegible]
R41	010123	RES, METAL, 23.7K, 1%, 1/8W	81349	[illegible]
R42	010125	RES, METAL, 16.2K, 1%, 1/4W	81349	[illegible]
R43	000470	RES, CARBON, 47 OHM, 5%, 1/4W	81349	[illegible]
R44	001881	RES, CARBON, 10 OHM, 5%, 1W	81349	[illegible]
R45	001881	RES, CARBON, 10 OHM, 5%, 1W	81349	[illegible]
R46	000681	RES, CARBON, 680 OHM, 5%, 1/4W	81349	[illegible]
R47	000432	RES, CARBON, 4.3K, 5%, 1/4W	81349	[illegible]
R48	010631	RES, METAL, 10.2K, 1%, 1/8W	81349	[illegible]
R49	000681	RES, CARBON, 680 OHM, 5%, 1/4W	81349	[illegible]
R50	000432	RES, CARBON, 4.3K, 5%, 1/4W	81349	[illegible]
R51	010631	RES, METAL, 10.2K, 1%, 1/8W	81349	[illegible]
R54	000681	RES, CARBON, 680 OHM, 5%, 1/4W	81349	[illegible]
R55	000681	RES, CARBON, 680 OHM, 5%, 1/4W	81349	[illegible]
R56	000510	RES, CARBON, 51 OHM, 5%, 1/4W	81349	[illegible]
R57	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	[illegible]
R58	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	[illegible]
R59	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D)   Figure 7-12   K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R60	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	RC07GF221J
R61	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R62	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R63	000822	RES, CARBON, 8.2K, 5%, 1/4W	81349	RC07GF822J
R64	001706	RES, CARBON, 510 OHM, 5%, 1/2W	81349	RC20GF511J
R65	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R66	000472	RES, CARBON, 4.7K, 5%, 1/4W	81349	RC07GF472J
R67	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R68	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R69	000510	RES, CARBON, 51 OHM, 5%, 1/4W	81349	RC07GF510J
R70	000510	RES, CARBON, 51 OHM, 5%, 1/4W	81349	RC07GF510J
R71	000132	RES, CARBON, 1.3K, 5%, 1/4W	81349	RC07GF132J
R72	000132	RES, CARBON, 1.3K, 5%, 1/4W	81349	RC07GF132J
R74	000471	RES, CARBON, 470 OHM, 5%, 1/4W	81349	RC07GF471J
R75	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R76	000474	RES, CARBON, 470K, 5%, 1/4W	81349	RC07GF474J
R77	000104	RES, CARBON, 100K, 5%, 1/4W	81349	RC07GF104J
R78	000123	RES, CARBON, 12K, 5%, 1/4W	81349	RC07GF123J
R79	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	RC07GF221J
R80	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	RC07GF221J
R81	000331	RES, CARBON, 330 OHM, 5%, 1/4W	81349	RC07GF331J
R82	000561	RES, CARBON, 560 OHM, 5%, 1/4W	81349	RC07GF561J
R83	000512	RES, CARBON, 5.1K, 5%, 1/4W	81349	RC-8GF512J

401725 - PCB ASSY., MOTHERBOARD (CONT'D)   Figure 7-12   K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R84	000560	RES, CARBON, 56 OHM, 5%, 1/4W	81349	[illegible]
R85	000471	RES, CARBON, 470 OHM, 5%, 1/4W	81349	RC07GF[illegible]
R86	000624	RES, CARBON, 620K, 5%, 1/4W	81349	[illegible]
R87	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF[illegible]
R88	000301	RES, CARBON, 300 OHM, 5%, 1/4W	81349	RC07GF3[illegible]
R89	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF[illegible]
R90	000153	RES, CARBON, 15K, 5%, 1/4W	81349	RC07GF15[illegible]
R91	000560	RES, CARBON, 56 OHM, 5%, 1/4W	81349	[illegible]
R92	000182	RES, CARBON, 1.8K, 5%, 1/4W	81349	RC07GF[illegible]
R93	000221	RES, CARBON, 220 OHM, 5%, 1/4W	81349	RC07GF2[illegible]
R94	000182	RES, CARBON, 1.8K, 5%, 1/4W	81349	RC07GF[illegible]
R95	000432	RES, CARBON, 4.3K, 5%, 1/4W	81349	RC07GF43[illegible]
R96	000511	RES, CARBON, 510 OHM, 5%, 1/4W	81349	RC07GF511[illegible]
R97	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R98	000471	RES, CARBON, 470 OHM, 5%, 1/4W	81349	RC07GF47[illegible]
R99	000202	RES, CARBON, 2K, 5%, 1/4W	81349	RC07GF20[illegible]
R100	000302	RES, CARBON, 3K, 5%, 1/4W	81349	RC07GF302J
R101	000912	RES, CARBON, 9.1K, 5%, 1/4W	81349	RC07GF912J
R102	000104	RES, CARBON, 100K, 5%, 1/4W	81349	RC07GF1[illegible]
R103	000103	RES, CARBON, 10K, 5%, 1/4W	81349	[illegible]
S1	600975	SWITCH, PUSHBUTTON	71590	SPEC-[illegible]
T1	300104	TRANSFORMER, PULSE	55167	[illegible]
U1	230547	IC, QUAD COMPARATOR	[illegible]	[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
U2	230746	IC, MEMORY, NON-VOL, 2K X 8	61394	5516A-300
U3	230731	IC, DIGITAL, NAND, DUAL QUAD INPUT	07263	74F20PC
U4	230719	IC, FAST NAND	07263	74F00
U5	230705	IC, DIGITAL	04713	74F04
U6	230744	IC, MICRO, 68000, 8 MHZ	04713	MC68000P8
U7	230740	IC, MEMORY, RAM, 8K, 150 NS	52531	HM6264P-15
U8	230740	IC, MEMORY, RAM, 8K, 150 NS	52531	HM6264P-15
U9	230368	IC, DEMULTIPLEXER	27014	74LS138
U10	230741	IC, INTERFACE, DAC, 12 BIT	24355	AD7545KN
U11	230743	IC, LINEAR, DUAL OP AMP	27014	LF412CN
U12	230742	IC, DIGITAL, PRIORITY ENCODER	04713	SN7545KN
U13	230637	IC, DIGITAL	18324	N74LS244
U14	230752	IC, LINEAR, OP AMP	24355	AD0P07CN
U16	921005	OSC, CLOCK, 8 MHZ, 0.1%	04713	RASCO-3
U17	230813	IC, MEMORY, 64K X 8	21793	230813
U18	230812	IC, MEMORY, 64K X 8	21793	230812
U19	230741	IC, INTERFACE, DAC, 12 BIT	24355	AD7545KN
U20	230745	IC, LINEAR, VOLTAGE REF, 5V	04713	MC1404V5
U22	230368	IC, DEMULTIPLEXER	27014	74LS138
U23	230752	IC, LINEAR, OP AMP	24355	AD0P07CN
U24	230711	IC, DIGITAL	07263	74F32
U25	230760	IC, DIGITAL	27014	MM74HC37
U26	230422	IC, OCTAL	34335	AM8304B
U27	230330	IC, TRI-STATE BUFFER	01295	74LS367

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
U28	230704	IC, DIGITAL TIMER	27014	[illegible]
U29	230386	IC, 8-BIT REGISTER	27014	[illegible]
U30	230637	IC, DIGITAL	18324	[illegible]
U31	230386	IC, 8-BIT REGISTER	27014	[illegible]
U32	230414	IC, QUAD EXCLUSIVE OR GATE	27014	[illegible]
U33	230315	IC, MULTIPLEXER	01295	[illegible]
U34	230386	IC, 8-BIT REGISTER	27014	[illegible]
U35	200294	TRANS, PNP, QUAD 40V	04713	[illegible]
U36	200294	TRANS, PNP, QUAD 40V	04713	[illegible]
U37	230711	IC, QUAD 2-INPUT OR GATE	04713	[illegible]
U38	230194	IC, 14 DIP, DUAL D FLIP-FLOP	01295	[illegible]
U39	230234	IC, 14 DIP, HEX INVERTER	01295	[illegible]
U40	230196	IC, 14 DIP, AND-OR-INV GATES	01295	[illegible]
U41	230507	IC, DIGITAL	27014	[illegible]
U42	230305	IC, QUAD, 2-INPUT AND GATES	01295	[illegible]
U43	230194	IC, 14 DIP, DUAL D FLIP-FLOP	01295	[illegible]
U44	230386	IC, 8-BIT REGISTER	27014	[illegible]
U45	200294	TRANS, PNP, QUAD 40V	04713	[illegible]
U46	230747	IC, LINEAR, VOLTAGE REG.	12969	[illegible]
U47	230747	IC, LINEAR, VOLTAGE REG.	12969	[illegible]
U48	230373	IC, VOLTAGE REGULATOR	04713	[illegible]
U49	230378	IC, 3-TERM NEG. REGULATOR	27014	[illegible]
U50	230442	IC, QUAD MTTL TO MECL TRANSL.	04713	[illegible]
U51	230443	IC, QUAD MECL TO MTTL TRANSL.	04713	[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
U52	230750	IC, DIGITAL, ECL	04713	MC10216P
U53	230443	IC, QUAD MECL TO MTTL TRANSL.	04713	MC10125
U54	230751	IC, DIGITAL, ECL	04713	MC10130P
U55	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231
U56	230442	IC, QUAD MTTL TO MECL TRANSL.	04713	MC10124
U57	230205	IC, QUAD 2, INPUT NOR GATE	04713	MC10102P
U58	230205	IC, QUAD 2, INPUT NOR GATE	04713	MC10102P
U59	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231
U60	230205	IC, QUAD 2, INPUT NOR GATE	04713	MC10102P
U61	230793	IC, DIGITAL, GPIB	01295	TMS9914ANL
U62	230445	IC, 686 VOLTAGE COMPARATOR	34335	AM686CN-1
U63	230748	IC, LINEAR, OP AMP	01295	TL081C
U64	230792	IC, LINEAR, TRANS ARRAY	02735	CA3046
U65	230509	IC, DIGITAL	27014	74LS132N
U66	230757	IC, LINEAR, 710 COMPARATOR	27014	MC1710CH
U67	230459	IC, OCTAL GPIB TRANS	01295	SN75160
U68	230472	IC, OCTAL GPIB TRANS	01295	SN75161
W1	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W2	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W3	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W4	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W6	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W7	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2
W8	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	531220-2

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
W9	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	[illegible]
W11	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	[illegible]
W12	601195	PLUG, JUMPER, 0.1 CTR, LOW PROFILE	00779	[illegible]
Y1	921004	OSC, 10 MHZ, CRYSTAL	55411	[illegible]
Z1	080005	RES NETWORK, CERMET, 10K, 6P5R, 2%	11236	[illegible]
Z2	080032	RES NETWORK, CERMET, 4.7K, 10P9R	11236	[illegible]
Z3	080015	RES NETWORK, 10K, 5%	91637	[illegible]
Z4	080023	RES NETWORK, 4.7K, 8P9R, 2%	11236	[illegible]
Z5	080067	RES NETWORK, 2.2K, 8 RES	11236	[illegible]
Z6	080035	RES NETWORK, 6K, 1.5W, 14P13R, 2%	11236	[illegible]
Z7	080067	RES NETWORK, 2.2K, 8 RES	11236	[illegible]
Z8	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	[illegible]
Z9	080080	RES NETWORK, 160 OHM, 8P7R	11236	[illegible]
Z10	080081	RES NETWORK, 270 OHM, 8P7R	11236	[illegible]
Z11	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	[illegible]
Z12	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	[illegible]
Z13	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	[illegible]
Z14	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	[illegible]

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Z15	080068	RES NETWORK, CERMET, 470 OHM, 3 RES	11236	750-63-R470 OHM
Z16	080002	RES NETWORK, 500 OHM, 8P7R, 2%	11236	750-81-R500 OHM
Z17	080005	RES NETWORK, 10K, 6P5R, 2%	11236	750-61-R10K OHM
215	500002	TUBING, SHRINK, .153 ID	—	—
216	600786	POST TERMINAL TP1-TP17, TP19-TP27, E1-E12, E25-E27, W6-W11 (2 EA) (53 REQ'D)	00779	1-87022-0
218	411725	PCB, MOTHERBOARD (UNLOADED)	21793	411725
220	600947	SOCKET, IC, 20P (2 REQ'D)	52072	CA-20S-TSD-BC
225	611059	CONNECTOR, DIP, LOW PROFILE, 40P	91506	240-AG39D
229	601199	SOCKET, 64P, LOW PROFILE	06776	ICA-649-S-TG
248	630010	KIT, HOWRE, STANDOFF, STUD MT	00779	552633-3
251	601230	HEATSINK, TO-220	13103	6232B-MT
255	610001	STANDOFF, 6-32 X 3/8, CAD PLATED BRASS (5 REQ'D)	88245	1530-B-3/8
257	610905	BRACKET, ANGLE, 8-32 TAPPED	79963	34S
258	610949	RIVET, .205D X .276L	19738	1601-5307
260	611065	SPACER, 14-PIN DIP	32559	814-100
261	615043	SCREW, PPH, 4-40 X .312	—	—

401725 - PCB ASSY., MOTHERBOARD (CONT'D) Figure 7-12 K

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
262	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (2 REQ'D)	78189	—
264	617004	NUT, HEX, 4-40	—	—
265	617077	WASHER, INT. LOCK, #4	—	—
268	920624	SOCKET, IC, 24P (2 REQ'D)	71785	133-29-02-[illegible]
272	920735	SOCKET, IC, 16P (2 REQ'D)	71785	133-5[illegible]-02-[illegible]
274	920891	SOCKET, 28P, SOLDER TAIL (4 REQ'D)	52072	CA-28S-TS[illegible]
278	920971	FUSEHOLDER, PC MOUNT (4 REQ'D)	75915	122088

401726 - PCB ASSY., SIGNAL CONDITIONER

Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1	100056	CAP, CERAM, 8.2 PFD, 1000V, 5%	56289	C0308102E8R2D
C2	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C3	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C4	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C5	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C6	100056	CAP, CERAM, 8.2 PFD, 1000V, 5%	56289	C0308102E8R2D
C7	100063	CAP, CERAM, .01 MFD, 500V, 20%	56289	C023B501E103M
C8	100063	CAP, CERAM, .01 MFD, 500V, 20%	56289	C023B501E103M
C9	100063	CAP, CERAM, .01 MFD, 500V, 20%	56289	C023B501E103M
C10	100063	CAP, CERAM, .01 MFD, 500V, 20%	56289	C023B501E103M
C11	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C12	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C13	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C14	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C15	101174	CAP, ELECT, 10000 MFD, 15V	80031	3050HS103U015
C16	101174	CAP, ELECT, 10000 MFD, 15V	80031	3050HS103U015
C17	130170	CAP, TRIMMER, .5-3 PFD, 300V	80031	2502A0R503VP02 F00
C18	130170	CAP, TRIMMER, .5-3 PFD, 300V	80031	2502A0R503VP02 F00
C19	130170	CAP, TRIMMER, .5-3 PFD, 300V	80031	2502A0R503VP02 F00

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D)

Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C20	130170	CAP, TRIMMER, .5-3 PFD, 300V	80031	[illegible] F00
C22	100050	CAP, CERAM, 2.2 PFD, 1000V, 5%	56289	C030[illegible]
C23	100050	CAP, CERAM, 2.2 PFD, 1000V, 5%	56289	[illegible]
C25	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C26	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C27	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C28	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C29	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C30	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C31	100146	CAP, CERAM, 39 PFD, 100V, 5%	05397	C315C3[illegible]
C32	130080	CAP, MICA, 22 PFD	72136	DM5F-2[illegible]
C33	130080	CAP, MICA, 22 PFD	72136	DM5E-2[illegible]
C34	100146	CAP, CERAM, 39 PFD, 100V, 5%	05397	C315C39[illegible]
C35	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C36	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C37	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
C38	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C39	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C40	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C41	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C42	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C43	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C44	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C45	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C46	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C47	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C48	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C49	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C50	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C51	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C52	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C53	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C54	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C55	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C56	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C57	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C58	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C59	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C60	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035[illegible]
C61	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C62	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C63	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C64	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C65	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C66	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035[illegible]
C67	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035[illegible]
C68	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C69	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C70	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035[illegible]
C71	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C72	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C73	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C74	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C75	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C76	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C77	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C78	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C79	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C80	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C81	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C82	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C83	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C84	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C85	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C86	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C87	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C88	130103	CAP, CERAM, .01 MFD, 25V, 20%	72982	GR42-6X7R103 M50Y
C89	130103	CAP, CERAM, .01 MFD, 25V, 20%	72982	GR42-6X7R103 M50Y
C90	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C91	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C92	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C93	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C94	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C95	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C96	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C97	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C98	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C99	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C100	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C101	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C102	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C103	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C104	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C105	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C106	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C107	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C108	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C109	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C110	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C111	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C112	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C113	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C114	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C115	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C116	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C117	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C118	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C119	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C120	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C121	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C122	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C123	110151	CAP, TANTA, 10 MFD, 35V, 20%	05397	T354G106M035AS
C124	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C125	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C126	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C127	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C128	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C129	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C130	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C131	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C132	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C133	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C134	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C135	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C136	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C137	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K
C138	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C139	130088	CAP, MICA, 5 PFD, 100V	72136	DM5D050-D0
C140	130088	CAP, MICA, 5 PFD, 100V	72136	DM5D050-D0
C141	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5R0-103K

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C142	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C143	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C144	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C145	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C146	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-W5RO-103K
C147	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C148	100147	CAP, CERAM, 120 PFD, 100V, 5%	05397	C315C121J1G5CA
C149	100147	CAP, CERAM, 120 PFD, 100V, 5%	05397	C315C121J1G5CA
CR1	210036	DIODE	07263	FD300
CR2	211083	DIODE, SILICO	81349	1N9168
CR3	211083	DIODE, SILICO	81349	1N9168
CR4	210036	DIODE	07263	FD300
CR5	210036	DIODE	07263	FD300
CR6	211083	DIODE, SILICO	81349	1N9168
CR7	211083	DIODE, SILICO	81349	1N9168
CR8	210036	DIODE	07263	FD300
CR9	210090	DIODE	50434	HP5082-2800
CR10	210090	DIODE	50434	HP5082-2800
CR11	210090	DIODE	50434	HP5082-2800
CR12	210090	DIODE	50434	HP5082-2800

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
J5	600823	SOCKET, DUAL IN-LINE, 40P	52072	[illegible]
J6	920734	SOCKET, IC, 14P	00779	583527-1
J7	601208-010	CONNECTOR, PCB PLUG, 2 PIN	21793	601208-010
J8	601208-010	CONNECTOR, PCB PLUG, 2 PIN	21793	601208-010
J101	601234	CONNECTOR, BNC, PCB MOUNT	21793	601234
J102	601234	CONNECTOR, BNC, PCB MOUNT	21793	601234
K1	310164	RELAY, REED, 1A, 200V	71707	2900-067
K2	310164	RELAY, REED, 1A, 200V	71707	2900-067
K3	310164	RELAY, REED, 1A, 200V	71707	2900-067
K4	310164	RELAY, REED, 1A, 200V	71707	2900-067
K5	310164	RELAY, REED, 1A, 200V	71707	2900-067
K6	310157	RELAY, CRYSTAL, CAN, 2P-2T	11532	172-12 [illegible]
K7	310157	RELAY, CRYSTAL, CAN, 2P-2T	11532	172-12 [illegible]
K8	310164	RELAY, REED, 1A, 200V	71707	2900-067
K9	310164	RELAY, REED, 1A, 200V	71707	2900-067
K10	310165	RELAY, REED, 2C	21317	[illegible]
K11	310164	RELAY, REED, 1A, 200V	71707	2900-067
K12	310163	RELAY, REED, 1C	14908	3420
K13	310163	RELAY, REED, 1C	14908	3420
L1	310092	CHOKE, RF, .1 UH	76493	9230-94
L2	310092	CHOKE, RF, .1 UH	76493	9230-94
L3	310056	CHOKE, RF, .68 UH	76493	9230-16
L4	310056	CHOKE, RF, .68 UH	76493	9230-16

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
L5	310056	CHOKE, RF, .68 UH	76493	9230-16
L6	310056	CHOKE, RF, .68 UH	76493	9230-16
L7	310056	CHOKE, RF, .68 UH	76493	9230-16
L8	310056	CHOKE, RF, .68 UH	76493	9230-16
L9	310056	CHOKE, RF, .68 UH	76493	9230-16
L10	310056	CHOKE, RF, .68 UH	76493	9230-16
L11	310056	CHOKE, RF, .68 UH	76493	9230-16
L12	310056	CHOKE, RF, .68 UH	76493	9230-16
L13	310056	CHOKE, RF, .68 UH	76493	9230-16
L14	310056	CHOKE, RF, .68 UH	76493	9230-16
L15	310056	CHOKE, RF, .68 UH	76493	9230-16
L16	310056	CHOKE, RF, .68 UH	76493	9230-16
P9	601213	CONNECTOR, EDGE, PLUG, 72 PIN	57856	PR36-6101-15
Q1	200297	TRANSISTOR, NPN	04713	MPS-H10
Q2	200291	TRANSISTOR, DMOS QUAD	17856	SD5000N
Q3	200291	TRANSISTOR, DMOS QUAD	17856	SD5000N
Q4	200197	TRANSISTOR, NPN	04713	MPS-H10
Q5	200197	TRANSISTOR, NPN	04713	MPS-H10
Q6	200197	TRANSISTOR, NPN	04713	MPS-H10
Q7	200099	TRANSISTOR, PNP	81349	2N4258
Q8	200290	TRANSISTOR, NPN	52648	SL3127C
Q9	200290	TRANSISTOR, NPN	52648	SL3127C
Q10	200099	TRANSISTOR, PNP	81349	2N4258

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Q11	200289	TRANSISTOR, DUAL, PNP	04713	MD5000A
Q12	200289	TRANSISTOR, DUAL, PNP	04713	MD5000A
Q13	200288	TRANSISTOR, FET, N-CHANNEL	17856	J105-18
Q14	200288	TRANSISTOR, FET, N-CHANNEL	17856	J105-18
R1	010137	RES, METAL 100 OHM, 1%, 1/4W	81349	RN60D[illegible]
R2	010137	RES, METAL 100 OHM, 1%, 1/4W	81349	RN60D[illegible]
R3	010137	RES, METAL 100 OHM, 1%, 1/4W	81349	RN60D[illegible]
R4	010137	RES, METAL 100 OHM, 1%, 1/4W	81349	[illegible]
R5	012123	RES, CERMET, 51 OHM, 1%, 1/4W	19647	MK132
R6	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF[illegible]
R7	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF[illegible]
R8	012123	RES, CERMET, 51 OHM, 1%, 1/4W	19647	MK132
R9	000680	RES, CARBON, 68 OHM, 5%, 1/4W,	81349	RC07GF68[illegible]
R10	000680	RES, CARBON, 68 OHM, 5%, 1/4W,	81349	RC07GF[illegible]
R11	010650	RES, METAL, 1M, 1%, 1/8W	81349	RN55C[illegible]
R12	010650	RES, METAL, 1M, 1%, 1/8W	81349	RN55[illegible]
R13	000510	RES, CARBON, 51 OHM, 5%, 1/4W	81349	RC07GF[illegible]
R14	000510	RES, CARBON, 51 OHM, 5%, 1/4W	81349	RC07GF51[illegible]
R15	000474	RES, CARBON, 470K, 5%, 1/4W	81349	RC07GF474J
R16	010536	RES, METAL, 100K, 1%, 1/8W	81349	RN55C[illegible]
R17	010536	RES, METAL, 100K, 1%, 1/8W	81349	RN55C[illegible]
R18	000474	RES, CARBON, 470K, 5%, 1/4W	81349	RC07GF[illegible]
R19	012110	RES, CERMET, 1.96M, 1%, 1/4W	19647	MK132
R20	012111	RES, CERMET, 1.8M, 1%, 1/4W	19647	MK132

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R21	012111	RES, CERMET, 1.8M, 1%, 1/4W	19647	MK132
R22	012110	RES, CERMET, 1.96M, 1%, 1/4W	19647	MK132
R23	012109	RES, CERMET, 41.67K, 1%, 1/4W	19647	MK132
R24	012108	RES, CERMET, 250K, 1%, 1/4W	19647	MK132
R25	012108	RES, CERMET, 250K, 1%, 1/4W	19647	MK132
R26	012109	RES, CERMET, 41.67K, 1%, 1/4W	19647	MK132
R27	000300	RES, CARBON, 30 OHM, 5%, 1/4W	81349	RC07GF300J
R28	000300	RES, CARBON, 30 OHM, 5%, 1/4W	81349	RC07GF300J
R29	000470	RES, CARBON, 47 OHM, 5%, 1/4W	80349	RC07GF470J
R30	000470	RES, CARBON, 47 OHM, 5%, 1/4W	80349	RC07GF470J
R31	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R32	012114	RES, METAL FILM, 316 OHM, 1%, 1/8W	81349	RN55C3160F
R33	012118	RES, METAL FILM, 1.5K, 1%, 1/8W	81349	RN55C1501F
R34	012118	RES, METAL FILM, 1.5K, 1%, 1/8W	81349	RN55C1501F
R35	012114	RES, METAL FILM, 316 OHM, 1%, 1/8W	81349	RN55C3160F
R36	012114	RES, METAL FILM, 316 OHM, 1%, 1/8W	81349	RN55C3160F
R37	012118	RES, METAL FILM, 1.5K, 1%, 1/8W	81349	RN55C1501F
R38	000105	RES, CARBON, 1M, 5%, 1/4W	81349	RC07GF105J
R39	012118	RES, METAL FILM, 1.5K, 1%, 1/8W	81349	RN55C1501F
R40	012114	RES, METAL FILM, 316 OHM, 1%, 1/8W	81349	RN55C3160F
R41	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R42	000105	RES, CARBON, 1M, 5%, 1/4W	81349	RC07GF105J
R43	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R44	010628	RES, METAL, 3.01K, 1%, 1/8W	81349	RN55C3011F

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R45	010628	RES, METAL, 3.01K, 1%, 1/8W	81349	RN55C3011F
R46	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R47	012121	RES, CERMET, 82.5 OHM, 1%, 1/4W	19647	MK120
R48	000122	RES, CARBON, 1.2K, 5%, 1/4W	81349	RC07GF122J
R49	012121	RES, CERMET, 82.5 OHM, 1%, 1/4W	19647	MK120
R50	000102	RES, CARBON, 1K, 5%, 1/4W	81349	RC07GF102J
R51	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R52	010918	RES, METAL, 499 OHM, 1%, 1/8W	81349	RN55C4990F
R53	012121	RES, CERMET, 82.5 OHM, 1%, 1/4W	19647	MK120
R54	012121	RES, CERMET, 82.5 OHM, 1%, 1/4W	19647	MK120
R55	010918	RES, METAL, 499 OHM, 1%, 1/8W	81349	RN55C4990F
R56	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R57	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R58	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R59	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R60	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C1000F
R61	012120	RES, CERMET, 1.5K, 1%, 1/4W	19647	MK120
R62	012122	RES, CERMET, 10 OHM, 1%, 1/4W	SEE NOTE 2 TABLE 7.1	LC-100
R63	012122	RES, CERMET, 10 OHM, 1%, 1/4W	SEE NOTE 2 TABLE 7.1	LC-100
R64	012120	RES, CERMET, 1.5K, 1%, 1/4W	19647	MK120
R65	012116	RES, METAL FILM, 475 OHM, 1%, 1/8W	81349	RN55C4750F
R66	012124	RES, METAL FILM, 301 OHM, 1%, 1/8W	81349	RN55C3010F
R67	040310	POT, CERMET, TOP ADJ, 1K, 10%	32997	3266W-1-1
R68	012115	RES, METAL FILM, 374 OHM, 1%, 1/8W	81349	RN55C3740F

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401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
R69	012084	RES, METAL FILM, 100 OHM, 1%, 1/8W	81349	RN55C10R0F
R70	040310	POT, CERMET, TOP ADJ, 1K, 10%	32997	3266W-1-102
R71	040310	POT, CERMET, TOP ADJ, 1K, 10%	32997	3266W-1-102
R72	010925	RES, METAL FILM, 1.33K, 1%, 1/8W	81349	RN55C1331F
R73	010704	RES, METAL, 1K, 1%, 1/8W	81349	RN55D1001F
R74	010704	RES, METAL, 1K, 1%, 1/8W	81349	RN55D1001F
R75	000161	RES, CARBON, 160 OHM, 5%, 1/4W	81349	RC07GF161J
R76	000161	RES, CARBON, 160 OHM, 5%, 1/4W	81349	RC07GF161J
R77	000271	RES, CARBON, 270 OHM, 5%, 1/4W	81349	RC07GF271J
R78	000271	RES, CARBON, 270 OHM, 5%, 1/4W	81349	RC07GF271J
R79	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R80	000680	RES, CARBON, 68 OHM, 5%, 1/4W	81349	RC07GF680J
R81	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
R82	001787	RES, CARBON, 20 OHM, 5%, 1/8W	81349	RC05GF200J
R83	001787	RES, CARBON, 20 OHM, 5%, 1/8W	81349	RC05GF200J
R84	000101	RES, CARBON, 100 OHM, 5%, 1/4W	81349	RC07GF101J
U1	230753	IC, DIGITAL, I & SENSITIVITY CONTROL	54473	3U15C13
U2	230753	IC, DIGITAL, I & SENSITIVITY CONTROL	54473	3U15C13
U3	230754	IC, LINEAR	01295	VA78L10ACLP
U4	230735	IC, COMPARATOR, DUAL ULTRA FAST	52648	SP9687DG
U5	230736	IC, INT., DUAL COMPARATOR	27014	LM2903N
U6	230750	IC, DIGITAL, ECL	04713	MC10216P
U7	230783	IC, ECL, HS QUAD 2-INPUT MUX	04713	MC10H158P
U8	230733	IC, DIGITAL, ECL FLIP-FLOP	04713	MC10231
U9	230750	IC, DIGITAL, ECL	04713	MC10216P

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
U10	230791	IC, DIGITAL	21793	230791
U11	230790	IC, DIGITAL	21793	230790
VR1	220007	DIODE, SILICO, ZENER	81349	1N751A
VR2	220007	DIODE, SILICO, ZENER	81349	1N751A
VR3	220007	DIODE, SILICO, ZENER	81349	1N751A
VR4	220098	DIODE, ZENER, 3.9V, 5%	04713	[illegible]
VR5	220098	DIODE, ZENER, 3.9V, 5%	04713	[illegible]
VR6	220098	DIODE, ZENER, 3.9V, 5%	04713	[illegible]
VR7	220098	DIODE, ZENER, 3.9V, 5%	04713	[illegible]
VR8	220101	DIODE, ZENER, 3.3V, 5%	04713	[illegible]
W1	601023	PLUG, JUMPER	98291	026-[illegible]
Z1	080069	RES NETWORK, CERMET, 2.2K, 3R	11236	750-63-R[illegible]
Z2	080068	RES NETWORK, CERMET, 470 OHM, 3R	11236	750-63-R47[illegible]
Z3	080068	RES NETWORK, CERMET, 470 OHM, 3R	11236	750-63-R[illegible]
Z4	080069	RES NETWORK, CERMET, 2.2K, 3R	11236	750-63-R2.2[illegible]
Z5	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R33[illegible]
Z6	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R33[illegible]
Z7	080065	RES NETWORK, CERMET, 33 OHM, 5R	11236	750-61-R33
Z8	080040	RES NETWORK, CERMET, 22K, 8P4R, 2%, 1.1W	11236	750-83-R2[illegible]
Z9	080039	RES NETWORK, CERMET, 100K, 6P3R, 2%, .9W	11236	750-63-R[illegible]
Z10	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R330
Z12	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R330
Z13	080001	RES NETWORK, CERMET, 330 OHM, 8P7R, 2%	11236	750-81-R330

401726 - PCB ASSY., SIGNAL CONDITIONER (CONT'D) Figure 7-25 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
Z14	080002	RES NETWORK, CERMET, 500 OHM, 8P7R, 2%	11236	750-81-R500
112	401728	PCB ASSY., MCC2 SYNCH	21793	401728
113	411726	PC BOARD, SIGNAL COND. (UNLOADED)	21793	411726
115	453936	RETAINER, FOAM, ADHESIVE	21793	453936
116	600786	POST, TERMINAL (TP5-12, W1 (2)) (10 REQ'D)	00779	1-87022-0
118	610912	CLIP, FLAT, CABLE	34785	031-0100
123	500022	WIRE, BARE COPPER, TRIMMED, SOLID, 22 GA	21793	500022
124	610227	NUT, PRESS, 2-56 (6 REQ'D)	46384	KF2-256
125	610612	STANDOFF, SWAGE, 4-40 X .453 (2 REQ'D)	06540	9536B-29-A0440-16
126	611032	SPACER, .2 CTR, .04 SHT, 2-LEAD (2 REQ'D)	32559	302-200
128	611043	WASHER, FLAT, #2, NYLON (2 REQ'D)	86928	5610-9-20
129	611059	CONNECTOR, DIP, LOW PROFILE, 40P	91506	240-AG-390
130	611060	CONNECTOR, DIP, LOW PROFILE, 16P (2 REQ'D)	91506	216-AG-390
132	615017	SCREW, PPH, 2-56 X .438 (2 REQ'D)	—	—
133	615019	SCREW, PPH, 2-56 X .625 (4 REQ'D)	—	—
134	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (2 REQ'D)	78189	—
135	617126	WASHER, LOCK, #2, LIGHT SERIES (4 REQ'D)	—	—
137	920563	BEADS, SHIELDING (8 REQ'D)	02114	56-590б5/4B
139	920962	LOCTITE, 242, MED STR.	05972	242

401728 - PCB ASSY., AMCC2 SYNCH Figure 7-33 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	[illegible] 103K
C2	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C3	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C4	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C5	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	[illegible] 103K
C6	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C7	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
C8	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C9	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-[illegible] 103K
C10	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
C11	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
C12	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
C13	100062	CAP, CERAM, .01 MFD, 100V, 10%	72982	8121-100-[illegible] 103K
Q1	200197	TRANSISTOR, NPN	04713	MPS-H10
Q2	200197	TRANSISTOR, NPN	04713	MPS-H10
Q3	200197	TRANSISTOR, NPN	04713	MPS-H10
Q4	200197	TRANSISTOR, NPN	04713	MPS-H10

401728 - PCB ASSY., AMCC2 SYNCH (CONT'D) Figure 7-33 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
U1	230787	IC, DIGITAL, TRIPLE LINE REC'R	04713	MC10116P
U2	230787	IC, DIGITAL, TRIPLE LINE REC'R	04713	MC10116P
U3	230442	IC, DIGITAL	04713	MC10124
U4	230785	IC, DIGITAL, TRIPLE X OR GATE	04713	MC10H107
U5	230787	IC, DIGITAL, TRIPLE LINE REC'R	04713	MC10116P
U6	230789	IC, DIGITAL, ECL/TTL CHIP	21793	230789
U7	230735	IC, COMPARATOR, DUAL ULTRA FAST	52648	SP9687DG
Z1	080075	RES NETWORK, CERMET, 470 OHM, 7R	11236	750-81-R470
Z2	080073	RES NETWORK, CERMET, 470 OHM, 5R	11236	750-61-R470
Z3	080073	RES NETWORK, CERMET, 470 OHM, 5R	11236	750-61-R470
Z4	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R330
Z5	080073	RES NETWORK, CERMET, 470 OHM, 5R	11236	750-61-R470
Z6	080075	RES NETWORK, CERMET, 470 OHM, 7R	11236	750-81-R470
Z7	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R330
Z8	080064	RES NETWORK, CERMET, 330 OHM, 5R	11236	750-61-R330
Z11	080004	RES NETWORK, CERMET, 4.7K, 6P5R, 2%	11236	750-61-R4.7K
Z12	080074	RES NETWORK, CERMET, 22K, 5R	11236	750-61-R22K
Z13	080004	RES NETWORK, CERMET, 4.7K, 6P5R, 2%	11236	750-61-R4.7K
Z14	080004	RES NETWORK, CERMET, 4.7K, 6P5R, 2%	11236	750-61-R4.7K
Z15	080074	RES NETWORK, CERMET, 22K, 5R	11236	750-61-R22K
19	411728	PCB, AMCC2, SYNCH (UNLOADED)	21793	411728
20	601019	CONNECTOR, TERM. STRIP, 20P, (2 REQ'D)	55322	TS-120-G-A1

401728 - PCB ASSY., AMCC2 SYNCH (CONT'D) Figure 7-33 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
21	611059	CONNECTOR, DIP, LOW PROFILE, 40P	91506	240-A[illegible]
22	611060	CONNECTOR, DIP, LOW PROFILE, 16P (3 REQ'D)	91506	216-A[illegible]

401727 - PCB ASSY., DISPLAY KEYBOARD

Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C2	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C3	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C4	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C5	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035AS
C6	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C7	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C8	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C9	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
C10	100133	CAP, CERAM, .1 MFD, LOW PROFILE, 20%	72982	8131LP-100-651-104M
CR1	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR2	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR3	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR4	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR5	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR6	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR7	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR8	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR9	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D)

Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
CR10	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR11	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR12	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR13	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR14	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR15	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR16	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR17	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR18	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR19	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR20	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR21	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR22	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR23	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR24	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR25	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR26	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR27	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR28	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR29	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR30	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR31	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR32	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR33	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D) Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
CR34	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR35	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR36	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR37	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR38	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR39	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR40	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR41	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR42	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR43	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR44	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR45	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR46	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR47	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR49	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR50	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR51	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR52	210106	DIODE, LIGHT EMITTING, RED	25088	LDH1112
CR53	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
CR54	210108	DIODE, LIGHT EMITTING, RED	25088	LDH5122
DS1	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS2	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS3	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS4	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D) Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
DS5	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS6	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS7	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-765[illegible]
DS8	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS9	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS10	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS11	210105	DISPLAY, NUMERIC, RED, R.H. DECIMAL	25088	DL-76510
DS12	210104	DISPLAY, 7 SEGMENT, 4 DIGIT	25088	DL340M
DS13	210104	DISPLAY, 7 SEGMENT, 4 DIGIT	25088	DL340M
P1	601223	CABLE ASSY., 34 CONDUCTOR	52072	CA-D34[illegible] 126/341032-3-00-003
R1	000561	RES, CARBON, 560 OHM, 5%, 1/4W	81349	RC07GF561J
R2	000561	RES, CARBON, 560 OHM, 5%, 1/4W	81349	RC07GF561J
R3	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R4	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R5	000561	RES, CARBON, 560 OHM, 5%, 1/4W	81349	RC07GF561J
R6	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
R7	000103	RES, CARBON, 10K, 5%, 1/4W	81349	RC07GF103J
S1	601211	SWITCH, PUSHBUTTON	21793	601211
S2	601211	SWITCH, PUSHBUTTON	21793	601211
S3	601211	SWITCH, PUSHBUTTON	21793	601211
S4	601211	SWITCH, PUSHBUTTON	21793	601211

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D) Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
S5	601211	SWITCH, PUSHBUTTON	21793	601211
S6	601211	SWITCH, PUSHBUTTON	21793	601211
S7	601211	SWITCH, PUSHBUTTON	21793	601211
S8	601211	SWITCH, PUSHBUTTON	21793	601211
S9	601211	SWITCH, PUSHBUTTON	21793	601211
S10	601211	SWITCH, PUSHBUTTON	21793	601211
S11	601211	SWITCH, PUSHBUTTON	21793	601211
S12	601211	SWITCH, PUSHBUTTON	21793	601211
S13	601211	SWITCH, PUSHBUTTON	21793	601211
S14	601211	SWITCH, PUSHBUTTON	21793	601211
S15	601211	SWITCH, PUSHBUTTON	21793	601211
S16	601211	SWITCH, PUSHBUTTON	21793	601211
S17	601211	SWITCH, PUSHBUTTON	21793	601211
S18	601211	SWITCH, PUSHBUTTON	21793	601211
S19	601211	SWITCH, PUSHBUTTON	21793	601211
S20	601211	SWITCH, PUSHBUTTON	21793	601211
S21	601211	SWITCH, PUSHBUTTON	21793	601211
S22	601211	SWITCH, PUSHBUTTON	21793	601211
S23	601211	SWITCH, PUSHBUTTON	21793	601211
S24	601211	SWITCH, PUSHBUTTON	21793	601211
S25	601211	SWITCH, PUSHBUTTON	21793	601211
S26	601211	SWITCH, PUSHBUTTON	21793	601211
S27	601211	SWITCH, PUSHBUTTON	21793	601211
S28	601211	SWITCH, PUSHBUTTON	21793	601211

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D) Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
S29	601211	SWITCH, PUSHBUTTON	21793	601211
S30	601211	SWITCH, PUSHBUTTON	21793	601211
S31	601211	SWITCH, PUSHBUTTON	21793	601211
S32	601211	SWITCH, PUSHBUTTON	21793	601211
S33	601211	SWITCH, PUSHBUTTON	21793	601211
S34	601211	SWITCH, PUSHBUTTON	21793	601211
S35	601211	SWITCH, PUSHBUTTON	21793	601211
S36	601211	SWITCH, PUSHBUTTON	21793	601211
S37	601211	SWITCH, PUSHBUTTON	21793	601211
S38	601211	SWITCH, PUSHBUTTON	21793	601211
S39	601211	SWITCH, PUSHBUTTON	21793	601211
S40	601211	SWITCH, PUSHBUTTON	21793	601211
S41	920905	SWITCH, MOMENTARY, SPST	31918	8151[illegible]
U1	230457	IC, LED DRIVER	50579	ICM7218A
U2	230457	IC, LED DRIVER	50579	ICM7218A
U3	230386	IC, DIGITAL	27014	74LS273
U4	230506	IC, INTERFACE 8-DIGIT LED DRIVES	32293	ICM7218B-[illegible]
U5	230386	IC, DIGITAL	27014	74LS273
U6	230386	IC, DIGITAL	27014	74LS273
U7	230636	IC, OCTAL BUFFER	18324	74LS244F
U8	230368	IC, DEMULTIPLEXER	27014	74LS138
Z1	080050	RES NETWORK, 470 OHM, 10P9R	11236	750-101-R4[illegible]
Z2	080023	RES NETWORK, CERMET, 4.7K, 8P7R, 2%	11236	750-81-R4.7K

401727 - PCB ASSY., DISPLAY KEYBOARD (CONT'D) Figure 7-36 F

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
26	411727	PCB, DISPLAY, KEYBOARD (UNLOADED)	21793	411727
29	454817	SPACER, LED, 7 POSITION (2 REQ'D)	21793	454817
30	454817-021	SPACER, LED, 3 POS. MOD.	21793	454817-021
31	454817-022	SPACER, LED, 4 POS. MOD.	21793	454817-022
39	611057	SPACER, LED, 1 POS. (7 REQ'D)	21793	611057
40	611065	SPACER, 14-PIN DIP (2 REQ'D)	32559	814-100
43	921007	CAP, SWITCH, GRAY (25 REQ'D)	21793	921007
44	921009	CAP, SWITCH, BLUE	21793	921009
46	921049-01	CAP, SWITCH, "1"	21793	921049-01
47	921049-02	CAP, SWITCH, "2"	21793	921049-02
48	921049-03	CAP, SWITCH, "3"	21793	921049-03
49	921049-04	CAP, SWITCH, "4"	21793	921049-04
50	921049-05	CAP, SWITCH, "5"	21793	921049-05
51	921049-06	CAP, SWITCH, "6" (2 REQ'D)	21793	921049-06
52	921049-07	CAP, SWITCH, "7"	21793	921049-07
53	921049-08	CAP, SWITCH, "8"	21793	921049-08
54	921049-09	CAP, SWITCH, "0"	21793	921049-09
55	921049-010	CAP, SWITCH, "."	21793	921049-010
56	921049-011	CAP, SWITCH, "EXP"	21793	921049-011
57	921049-012	CAP, SWITCH, "CE"	21793	921049-012
58	921049-013	CAP, SWITCH, "+/-"	21793	921049-013

404331 - ASSY., REAR PANEL Figure 7-39 E

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
B200	921015	FAN, DC, 20 CFM, 2.38 SQ	21793	921015
C200	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035-
C201	110126	CAP, TANTA, 6.8 MFD, 35V, 20%	05397	T355F685M035-
CR200	230594	IC, FULL WAVE RECT. BRIDGE	27777	VH148
J211	601219	CONNECTOR, PWR, EMI FILTER	05245	6J4
P11	601215	CONNECTOR, PWR, HOUSING, 15P	00779	1-350244-9
P13	601216	CONNECTOR, PWR, HOUSING, 6P	00779	1-350243-9
P20	611055	CONNECTOR, CABLE, 4 PIN	00779	530554-3
Q200	200301	TRANSISTOR, PNP, PWR, 75W	04713	MJE2955T
Q201	200302	TRANSISTOR, NPN, PWR, 75W	04713	MJE3055T
S200	601112	SWITCH, ROCKER, DPST	NOTE 3 TABLE 8.1	1555.1102
U200	230788	IC, LINEAR, V REG	04713	LM340AT-5.0
2	404331-001	ASSY., REGULATOR	21793	404331-001
5	404331-002	ASSY., POWER RECPTLE	21793	404331-002
10	454592	BOOT, CONN. INSULATOR	21793	454592
11	454763	PANEL, REAR	21793	454763
13	454822-020	HOUSING, FAN, STD.	21793	454822-020
14	454823	GUARD, FINGER, FAN	21793	454823
15	454824	HEATSINK, BRKT, RIGHT	21793	454824
16	454825	HEATSINK, BRKT, LEFT	21793	454825

404331 - ASSY., REAR PANEL (CONT'D) Figure 7-39 A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
17	522222	WIRE, TEFLON, STR, 18G, RED	—	—
18	500052	WIRE, TEFLON, STR, 18G, BLK	—	—
19	500061	WIRE, TEFLON, STR, 18G, WHT	—	—
20	500064	TUBING, SHRINK, .09310, BLK	—	—
21	522333	WIRE. TEFLON, STR, 18G, ORG	—	—
22	500070	WIRE, TEFLON, STR, 18G, BLK/RED	—	—
23	500071	WIRE, TEFLON, STR, 18G, BLK/ORG	—	—
24	500074	WIRE, TEFLON, STR, 18G, WHT/ORG	—	—
25	522244	WIRE, TEFLON, STR, 18G, YEL	—	—
26	500212	WIRE, TEFLON, STR, 18G, GRN	—	—
27	500214	WIRE, TEFLON, STR, 18G, BRN	—	—
28	500215	WIRE, TEFLON, STR, 18G, GRN/YEL	—	—
29	500216	WIRE. TEFLON, STR, 18G, BLU	—	—
30	522777	WIRE, TEFLON, STR, 18G, VIO	—	—
31	600022	LUG, SOLDER	83330	1416-6
33	600745	TERMINAL, RECEPTACLE	00779	60196-3
35	601011	TERMINAL, CRIMP, .039 DIA	00779	60059-2
38	601212	TERMINAL, CRIMP, 18-26	00779	641294-1
44	610777	CABLE TIE	53421	T18R
46	610820	WASHER, SHOULDER, TO-220	13103	14875
48	610851	WASHER, INSULATING, TIP-32 STYLE	18565	60-11-5791-1674
49	610889	SCREW. PPH, 4-40 X .375	—	—
50	500056	TUBING, CLR, 3/16" DIA	—	—
51	611052	KEY, POLARIZING, PLUG	00779	87077-1

404331 - ASSY., REAR PANEL (CONT'D) Figure 7-39 A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
52	611053	TERMINAL. CRIMP (2 REQ'D)	00779	530553-?
55	615068	SCREW, PPH, 6-32 X 1.50 (4 REQ'D)	—	—
57	616252	SCREW, PPH, SEMS ASSY., 4-40 X .312 (4 REQ'D)	78189	—
59	617005	NUT, HEX, 6-32	—	—
61	617103	WASHER. FLAT, #6, LIGHT SERIES (4 REQ'D)	—	—
63	617128	WASHER, LOCK, #6, LIGHT SERIES (4 REQ'D)	—	—
65	920364	FUSE. SLO BLO, 1A	75915	313.001?

404378 - ASSY., REAR INPUT (OPT. 01)

Figure 7-40 A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	401752	PCB ASSY., REAR INPUT	21793	401752
5	601222	CABLE ASSY., 72 CONDUCT	21793	601222
7	611058	STANDOFF, 6-32 X 1.25 (5 REQ'D)	06540	8224-SS-0632-F
9	616255	SCREW, PPH, SEMS ASSY (9 REQ'D)	21793	616255

401752 - PCB ASSY., REAR INPUT

Figure 7-41 B

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	411752	PCB, REAR INPUT (UNLOADED)	21793	411752
4	601213	CONNECTOR, EDGE, PLUG 72 PIN (2 REQ'D)	57856	PR36-6141-15
6	610227	NUT, PRESS, 2-56 (4 REQ'D)	46384	KF2-256
8	615017	SCREW, PPH, 2-56 X .438 (4 REQ'D)	—	—
9	920962	LOCTITE, 242, MED STR	05972	242
10	610198	WASHER, FLAT, NYLON, #4 (4 REQ'D)	86928	5610-10-31

404384 - OPT. 04E, OSCILLATOR Figure 7-42 C

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
3	404386	OSCILLATOR ASSY	21793	404386
5	610777	CABLE TIE	53421	118R
7	611067	SCREW, METRIC, M3 X 8 (2 REQ'D)	—	—
9	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	—	—
10	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	—	—

404386 - OSCILLATOR ASSY. (OPT. 04E) Figure 7-43 C

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
J4	611056	CONNECTOR, CABLE, 5-PIN	21793	611056
1	401822	PCB ASSY, DOUBLER	21793	[illegible]
2	454879	FREQUENCY STD, 5 MHZ	21793	[illegible]
4	500064	TUBING, SHRINK, .093 ID	—	—
6	610304	SPACER, 1/4 D X 1/2 LG (2 REQ'D)	—	—
8	611074	SCREW, METRIC, M3 X 10 (2 REQ'D)	—	—
10	617102	WASHER, FLAT, #4, LIGHT SERIES (2 REQ'D)	—	—
11	617127	WASHER, LOCK, #4, LIGHT SERIES (2 REQ'D)	—	—
13	500009	TUBING, SHRINK, .125 ID, BLK	29005	RNF-100-1-1/8
15	500174	CABLE, COAX, LOW THERMAL	21793	500174
17	524555	WIRE, TEFLON, STRANDED, 24 GA, GRN	—	
18	524929	WIRE, TEFLON, STRANDED, 24 GA, WHT/RED	—	
20	610777	CABLE TIE	53421	T18R
22	611052	KEY, POLARIZING, PLUG	00779	87077-1
23	611053	TERMINAL, CRIMP	00779	530553-2

Figure 7-44 A

401822 - PCB ASSY., DOUBLER

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
C1-9	R-21-1801	CAP, CHIP, 10NF	95275	VJ1206Y103MF
D1-2	R-22-1029	DIODE, SILICON	14433	1N4149
L1	310151	CHOKE, 10%, 100 UH	83125	DD1000H
Q1-2	200299	TRANS, PNP	04713	2N3906
Q3-5	200298	TRANS, NPN	04713	2N3904
R1	R-20-5776	RES, CHIP, 33 OHM, 1/8W, 5%, 200V	65940	MCR18-33 OHM-5%
R2-3	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	65940	MCR18-100 OHM-5%
R4	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR19-1K-5%
R5-6	R-20-5785	RES, CHIP, 470 OHM, 1/8W, 5%	65940	MCR18-470 OHM-5%
R7	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	65940	MCR18-1.5K-5%
R8-9	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5%, 200V	65940	MCR18-3.9K-5%
R10	R-20-5794	RES, CHIP, 1.5K, 1/8W, 5%, 200V	65940	MCR18-1.5K-5%
R11	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5%
R12	R-20-5808	RES, CHIP, 39K, 1/8W, 5%, 200V	65940	MCR18-39K-5%
R13	R-20-5803	RES, CHIP, 15K, 1/8W, 5%, 200V	65940	MCR18-15K-5%
R14	R-20-5816	RES, CHIP, 330K, 1/8W, 5%, 200V	65940	MCR18-330K-5%
R15	R-20-5768	RES, CHIP, 10K, 1/8W, 5%, 200V	65940	MCR18-10K OHM-5%
R16	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5%
R17-18	R-20-5798	RES, CHIP, 3.9K, 1/8W, 5%, 200V	65940	MCR18-3.9K-5%
R19	R-20-5764	RES, CHIP, 100 OHM, 1/8W, 5%	65940	MCR18-100 OHM-5%
R20	R-20-5792	RES, CHIP, 1K, 1/8W, 5%, 200V	65940	MCR18-1K-5%
R21	R-20-5814	RES, CHIP, 51 OHM, 1/8W, 5%, 200V	65940	MCR18-51 OHM-5%
T1-2	R-23-7149	TRANSFORMER	21793	R-23-7143
TP1	R-24-3537	TERMINAL ASSY.	21793	R-24-3537
10	411822	PCB, DOUBLER (UNLOADED)	21793	411822
58	R-24-3519	AV LUGS (3 REQ'D)	19738	AVLUG1107/0208

404387 - 220V/240V OPERATION (OPT. 71). A

REF DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	920204	FUSE, SLO BLO, .50A., 250V	75915	[illegible]

404293 - BOTTOM COVER ASSEMBLY Figure 7-48

REF. DESIG.	RACAL-OANA P/N	DESCRIPTION	FSC	MFG. P/N
1	454351	BAIL	21793	454351
2	454354	COVER	21793	454354
3	920958	RIVET (4 REQ'D)	98388	3188
4	454355	PAD, FOOT (4 REQ'D)	21793	454355
5	920504	ADHESIVE, SCOTCH GRIP	04963	4475
6	454621	FOOT (4 REQ'D)	21793	454621
7	610554	SCREW, TAP, #8-18x3/8, TYPE B (4 REQ'D)	08226	PTH-8-18x3/8-SS-BLK
8	454542	PLATE (4 REQ'D)	21793	454542

404183 - RACK SLIDE KIT Figure 7-49

REF. DESIG.	RACAL-DANA P/N	DESCRIPTION	FSC	MFG. P/N
1	454597	RETAINER, COVER (2 REQ'D)	21793	454597
2	454488	KIT, BRACKET (INCLUDES ITEMS 6 THRU 10)	21793	454488
3	610920	NUT, RETAINER (8 REQ'O)	21793	610920
4	615091	SCREW, PPH, 10-32x.500 (8 REQ'D)	21793	615091
5	454489	SLIDE (2 REQ'D)	21793	454489
6	--	SCREW, PPH, 8-32x.375 (8 REQ'D)	969D6	MS35206-243
7	--	BRACKET (4 REQ'D)	05236	SP0551
8	--	NUT, #8-32 (8 REQ'D)	96906	MS35649-282
9	--	WASHER, LOCK , #8 (8 REQ'D)	96906	MS35338-42
10	--	WASHER, FLAT, #8 (8 REQ'D)	88044	AN960-8
11	610910	SCREW, PPH, 8-32x.312 (8 REQ'D)	21793	610910
12	615325	SCREW, PFH, 8-32x.500 (4 REQ'D)	21793	615325
13	610921	WASHER, FLAT, #8 (2 REQ'D)	21793	610921
14	454422	EAR, MOUNTING (2 REQ'D)	21793	454422
15*	615093	SCREW, PPH, 10-32x.750 (4 REQ'D)	21793	615093
15*	611011	SCREW, PFH, M4x12 (4 REQ'D)	21793	611D11
16	454490	MOUNTING BLOCK, SLIDE (6 REQ'D)	21793	454490
17	454323	INSERT, CORNER (2 REQ'D)	21793	454323

*For Ref. Desig. 15, use screw with English or metric dimensions as appropriate.

AMENDMENT

Racal-Dana Model 1995/1996
Instruction Manual
Publication No. 980599
January 5, 1989

1. Add the following subassemblies to the Drawings section:

   a. Insert Change Page 7-48, 404293, Bottom Cover Assembly.

   b. Insert Change Page 7-49, 404183, Rack Slide Kit.

2. Add the following Parts Lists for the above two assemblies:

   a. Insert Change Page 8-39, 404293, Bottom Cover Assembly.

   b. Insert Change Page 8-40, 404183, Rack Slide Kit.

3. Page 7-9. Schematic, Channel C (Zone D4-6):

   a. Change "L2" to "R9".

   b. Change "L3" to "R11".

   c. Change "L4" to "R15".

4. Page 8-5, 404332 Chassis Parts List:

   a. Ref(erence) Desig(nator) "9" should be "4".

   b. Ref(erence) Desig(nator) "12":

      Change Racal-Dana and Manu(facturers) P/N to "454762".

   c. Ref(erence) Desig(nator) "14":

      Change Racal-Dana and Manu(facturers) P/N to "454765".

5. Page 8-6, 404389 Channel C Parts List:

   Ref(erence) Desig(nator) C23:

   a. Change Racal-Dana P/N to "R-21-1788".

   b. Change Manu(facturers) P/N to "VJL206A120JF".

6. Page 8-7, 404389 Channel C Parts List:

Ref(erence) Desig(nator)s R9 and R11:

a. Change Racal-Dana P/N to "R-20-5786".

b. Change resistor value to "270 ohm".

c. Change Manu(facturers) P/N to "MCR18-270-5PCT".

7. Page 8-16, 401725 Motherboard Parts List:

Add R52 and R53, Racal-Dana P/N 000511,

RES, CARBON, 510 ohm, 5%, 1/4 W,

FSC: 81349 MFG. P/N: RC07GF511J

8. Page 8-37, 404386, Oscillator Assembly Parts List:

Ref(erence) Desig(nator) "J4" should be "J14".

9. Page 8-38, 401822, Doubler Parts List:

Ref(erence) Desig(nator) "58" should be "68".

404469 OSC , RUBIDIUM STAND. OPTION 04R

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
J23	600545	PLUG, 3 PIN	27264	1625-3P-1
P21	601216	CONNECTOR, PWR, HOUSING, 6 PIN	00779	1-35-0241-9
{1}1	401858	PCB ASSY, RUBIDIUM OSC. P.S.	21793	401858
{3}1	404565	MODULE ASSY, RUBIDIUM OSCILLATOR	21793	404565
{5}1	455187	MOUNTING BRACKET, RUBIDIUM OSC.	21793	455187
{6}1	455189	MOUNTING PLATE, POWER SUPPLY	21793	455189
{8}A/R	500002	TUBING, SHRINK, .187 ID	8C945	M23053/5-105-0
{9}A/R	500133	CABLE, SHIELDED, 22GA, 3 COND.	70903	8771
{11}A/R	520111	WIRE, TEFLON STRANDED, 20G,	-	-
{12}A/R	520333	WIRE, TEFLON STRANDED, 20GA, BRN	-	-
{13}A/R	520444	WIRE, TEFLON COATED, STRANDED, 20GA, YEL	-	-
{14}A/R	520555	WIRE, TEFLON STRANDED, 20 GA, GRN	---	---
{16}3	600380	THERMINAL PIN, MALE, .062 (3 REQ'D)	27264	1854
{19}5	601212	TERMINAL, CRIMP, 18-26	00779	641294-1
{21}3	601696	WIRE SPLICE, 22-18GA (3 REQ'D)	53387	558
{23}4	610777	CABLE TIE	16956	08-432
{26}4	615045	SCREW, PPH, 4-40X.437	-	-
{28}4	615556	SCREW, PFH, 6-32 X .250	---	---
{30}6	616252	SCREW, PPH, SEMS ASSY, 4-40X.312	78189	63-040545-25
{32}4	617102	WASHER, FLAT, #4, LIGHT SERIES	-	-
{34}4	617127	WASHER, LOCK, #4, LIGHT SERIES	-	-

404565 MODULE ASSY, RU OSC

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
P23	600379	RECEPTACLE, 3-PIN	27264	1625-3R
{1}1	455185	HEAT SINK, RUBIDIUM OSC.	21793	455185
{2}2	455186	COVER, RUBIDIUM OSC. HOUSING (2 REQ'D)	21793	455186
{3}2	455188	SIDE PLATE, OSC. HOUSING (2 REQ'D)	21793	455188
{5}A/R	500002	TUBING, SHRINK, .187 ID	8C945	M23053/5-105-0
{6}A/R	500064	TUBING, SHRINK, .093 ID, BLK	29005	RNF-100-1-3/32
{7}A/R	500254	CABLE, COAXIAL, 50 OHM	92194	9178B
{9}A/R	520111	WIRE, TEFLON STRANDED, 20G,	-	-
{10}A/R	520333	WIRE, TEFLON STRANDED, 20GA, BRN	-	-
{11}A/R	520444	WIRE, TEFLON COATED, STRANDED, 20GA, YEL	-	-
{12}A/R	520555	WIRE, TEFLON STRANDED, 20 GA, GRN	---	---
{15}3	600381	TERMINAL PIN, FEMALE, .062 (3 REQ'D)	27264	02-06-1855
{17}4	610777	CABLE TIE	16956	08-432
{19}1	611052	KEY, POLARIZING, PLUG	00779	87077-1
{20}2	611053	TERMINAL, CRIMP	00779	530553-2
{21}1	611056	CONNECTOR, CABLE, 5-PIN	21793	611056
{22}1	611178	TIE WRAP, SCREW MOUNT	06915	W1TS-18MR
{24}2	615047	SCREW, PPH, 4-40 X .625 (2 REQ'D)	-	-
{26}4	615541	SCREW, PFH, 4-40X.250	-	-
{27}8	615543	SCREW, PFH, 4-40X.375	-	-
{29}4	615705	SCREW, PFL, 4-40 X .500 (4 REQ'D)	-	-
{31}2	617102	WASHER, FLAT, #4, LIGHT SERIES	-	-
{33}6	617127	WASHER, LOCK, #4, LIGHT SERIES	-	-
{35}A/R	920469	THERMAL JOINT COMPOUND	13103	250
{37}1	921090	RUBIDIUM OSCILLATOR	55761	FRS-814-102-1

401858 PCB ASSY,-RU OSC PWR SUPPLY

REF DESIG	RACAL-DANA P/N	DESCRIPTION	FSC	MANUFACTURER'S P/N
C1	110225	CAP, AL. ELECT., 2200 UF, 50V	05397	SME50T222M18X40LL
C2	110225	CAP, AL. ELECT., 2200 UF, 50V	05397	SME50T222M18X40LL
C3	110126	CAP, TANTA, 6.8UF, 35V, 20 PERCENT	05397	T355F685M035AS
C4	110143	CAP, TANTA, 1 UF, 35V, 20 PERCENT	05397	T355A105M035AS
CR1	210004	DIODE, SILICON	81349	1N4004
CR2	210004	DIODE, SILICON	81349	1N4004
CR3	210004	DIODE, SILICON	81349	1N4004
CR4	210004	DIODE, SILICON	81349	1N4004
CR5	210004	DIODE, SILICON	81349	1N4004
CR6	210004	DIODE, SILICON	81349	1N4004
J21	601218	CONNECTOR, PWR, PLUG, 6-PIN	00779	9-350258-1
R1	000241	RES, CARBON, 240 OHM, 5 PERCENT, 1/4W	81349	RC07GF241J
R2	001275	RES, CARBON, 3.3K, 1/2W, 5PCT	81349	RC20GF332J
R3	040260	POT, CERMET, 1K, 20PCT	73138	72XW1K
T1	300106	TRANSFORMER, 24V, 2A	95075	L050-1-524
U1	230982	IC, LINEAR, 338 REGULATOR	27014	LM338K
{9}4	610777	CABLE TIE	16956	08-432
{11}1	411858	PCB, RUBIDIUM OSC P.S.(UNLOADED)	21793	411858
{12}1	600796	HEATSINK, TESTER, T03-T066	53894	425GI
{13}1	600842	INSULATOR, MICA	91833	4653
{14}A/R	500009	TUBING, SHRINK, .12 ID, BLK	29005	RNF-100-1-1/8
{16}4	610533	NUT, PRESS, 6-32, SPLINE (4REQ'D)	46384	KF2-632
{17}2	610899	TIE, CABLE, SELF-LOCKING, 1/16X2	58730	TY-232M
{19}2	615058	SCREW, PPH, 6-32 X .312	---	---
{20}2	615059	SCREW, PPH, 6-32 X .375	---	---
{21}4	617115	WASHER, FLAT, #6 (4 REQ'D)	-	-
{22}4	617128	WASHER, LOCK, #6, LIGHT SERIES	-	-
{23}A/R	920469	THERMAL JOINT COMPOUND	13103	250
{24}1	920804	LABEL, HIGH VOLTAGE	21793	920804

AMENDMENT

SLIDE RACK-MOUNT KIT INSTALLATION INSTRUCTIONS

NOVEMBER, 1987

In recent slide rack-mount kits, the front and rear rack-brackets are the same size and each has only one screw slot. Otherwise, the installation procedure remains as described in the manual.

AMENDMENT

RACAL-DANA MODEL 1995/6. PUBLICATION NO. 900599

RACAL-DANA MODEL 1995/6-02M. PUBLICATION NO. 980607

February 3, 1989

1. Add to Table 7.1 - List of Supplies

   FSC : 34649
   NAME : Intel
   Santa Clara, CA

2. Correct Motherboard Parts List (401725 & 401725-02M) FSC and Mfg. P/N for U28.

   FSC : 34649
   MFG. P/N : 8254-2

AMENDMENT TO

1995/6 INSTRUCTION MANUAL
PUBLICATION NO. 980599

April 28, 1989

1. Page 8-18, Correct manufacturers part number for U12.
Should be: SN74LS148N

AMENDMENT

to the 1995/6 and 1995/6-02M Instruction Manuals
Part numbers 980599 and 980607

June 14, 1989

This Amendment adds the Rubidium Frequency Standard, Option 04R, part number 404469.

Drawings included in this amendment:

404469 – Assembly, Rubidium Standard

404565 – Module Assembly, Rubidium Oscillator

401858 – PCB Assy., Rubidium Oscillator Power Supply
431858 – Schematic, Rubidium Oscillator Power Supply

Calibration Procedure on following page.

<u>Option 04R Calibration Procedure</u>

1) Connect equipment as shown in Figure 1.1

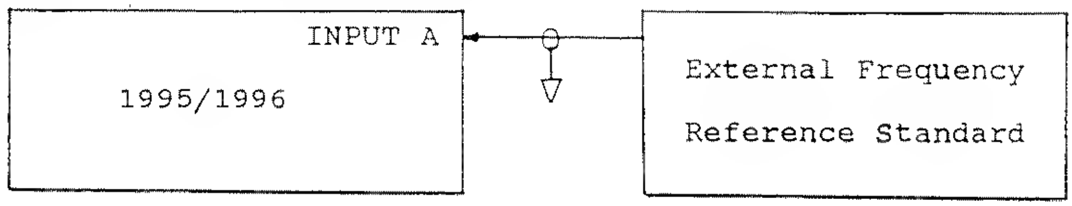


Figure 1.1

<u>Counter Input/Control Settings</u>

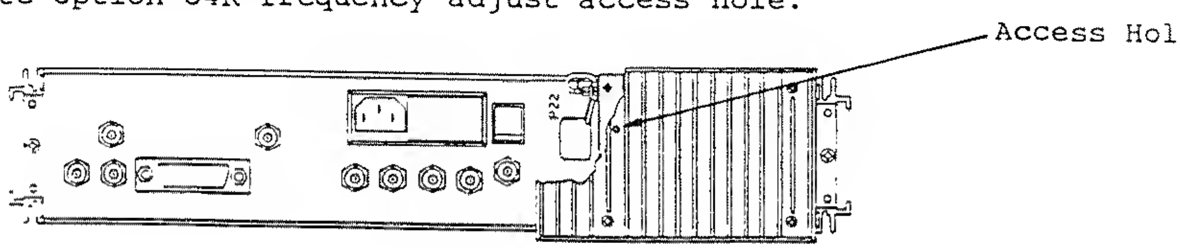
a) Select FREQ A
b) Select AC coupling, Input A
c) Select 50 ohms impedance, Input A
d) Set gate time of 100Sec

2) Allow sufficient time for equipment to stabilize

Note

Option 04R requires 4 minutes stabilization to obtain the following frequency accuracy: ±1x10E-9 of the final frequency(calibrated frequency), or the frequency before turn off, (if turn off was within 24 hours). The frequency will typically be within ±2x10E-11 of the final frequency after 1 hour. If the unit was not recently calibrated, the maximum frequency offset after one hour of operation would be: ±2x10E-11 warmup accuracy, ±2x10E-11 retrace. This assumes the last calibration was at the same ambient temperature.

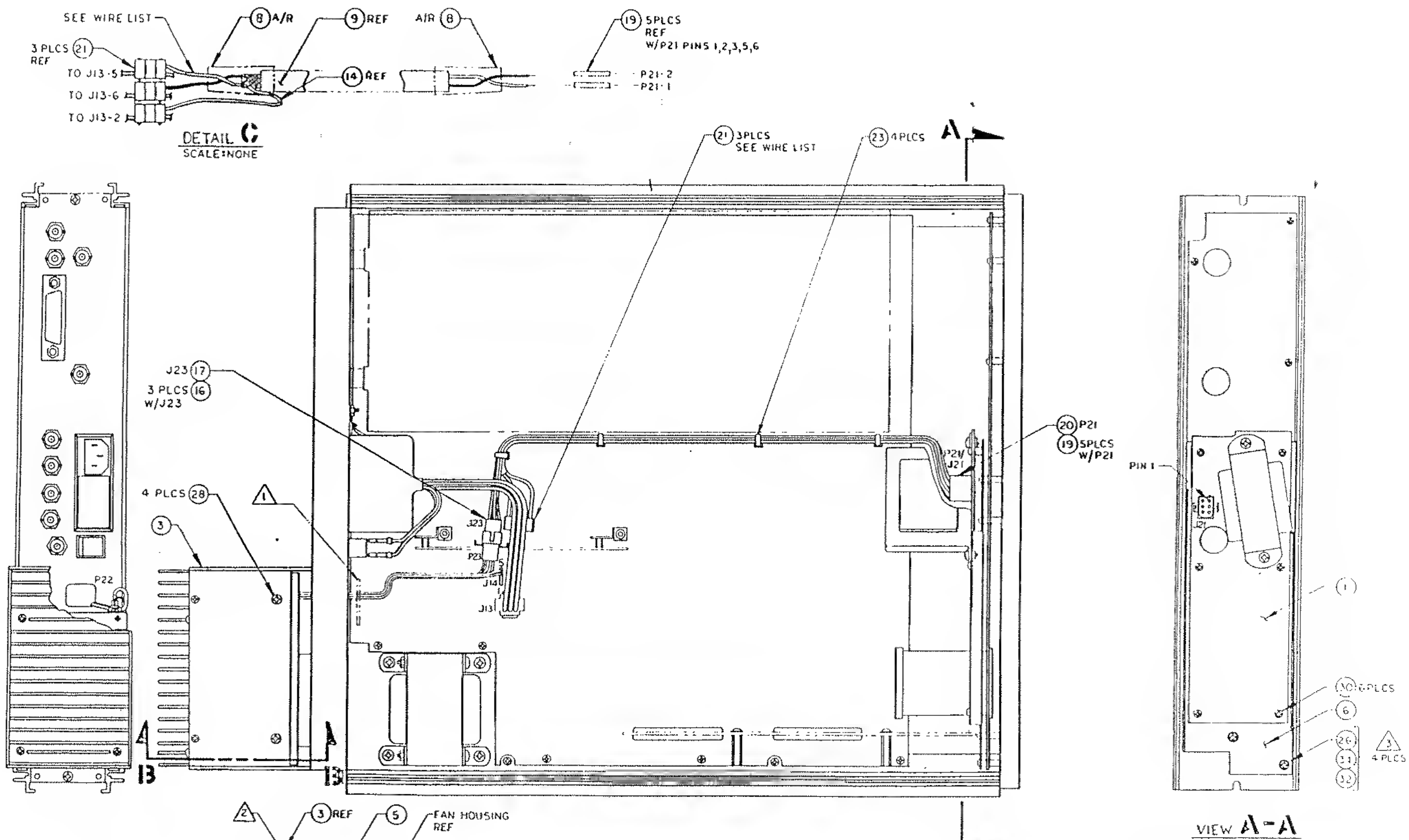
3) Locate Option 04R frequency adjust access hole.

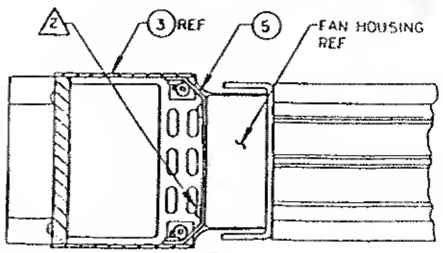


Note

The frequency of Option 04R may be adjusted over a range of approximately ±2x10E-9 by means of a 10 turn potentiometer accessible through the frequency adjust access hole.

4) Using a small screwdriver, slowly adjust the potentiometer while watching the counter display. Adjust the unit's output to the External Frequency Reference Standard ±5x10E-11 Hz.





SECTION B-B

3. REPLACE EXISTING HARDWARE WITH HARDWARE NOTED TO ATTACH MTG PLATE (ITEM #6).

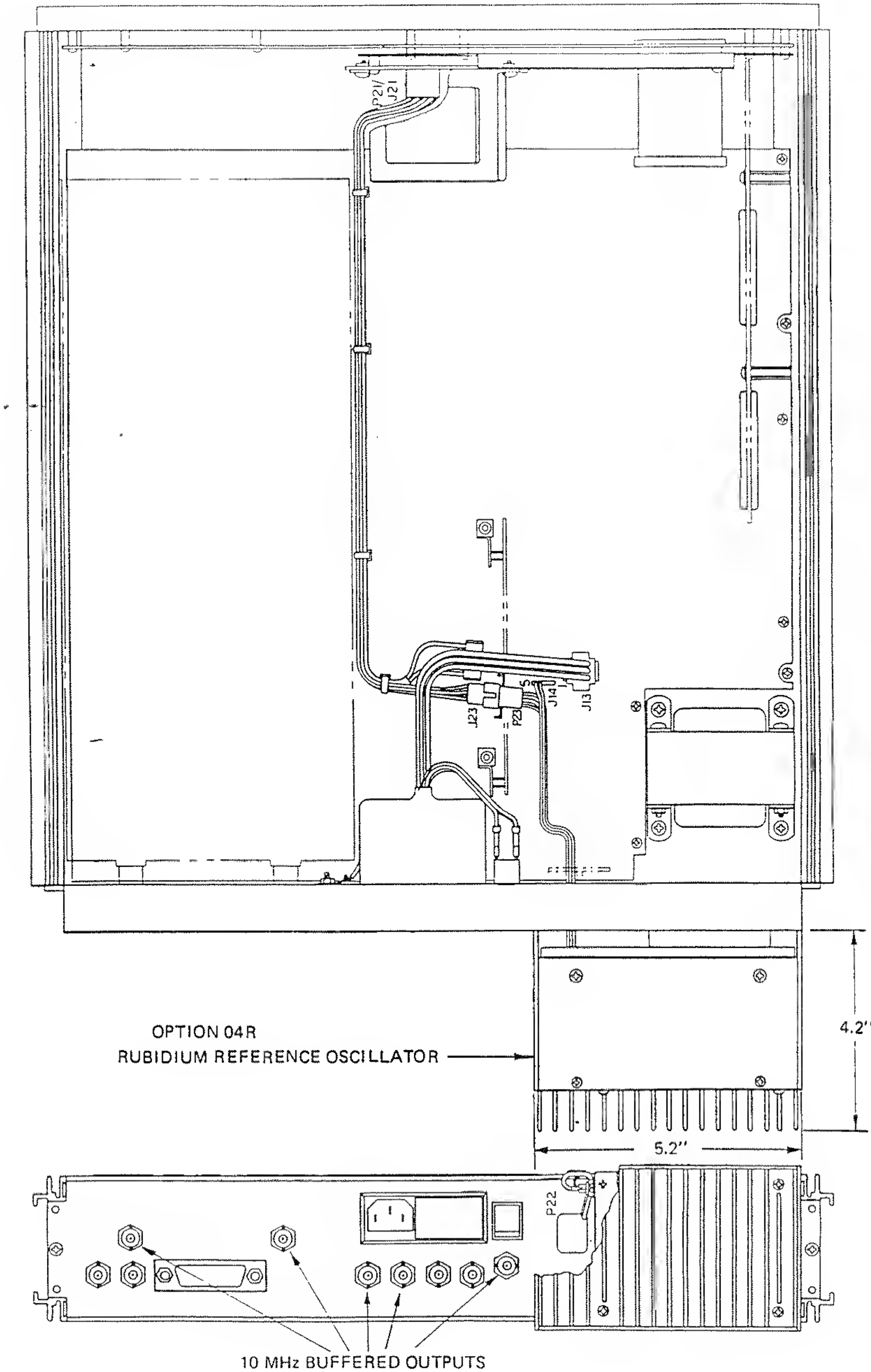
2. USE FAN MOUNTING SCREWS TO ATTACH OSCILLATOR MTG BRKT (ITEM #5) TO FAN HOUSING.

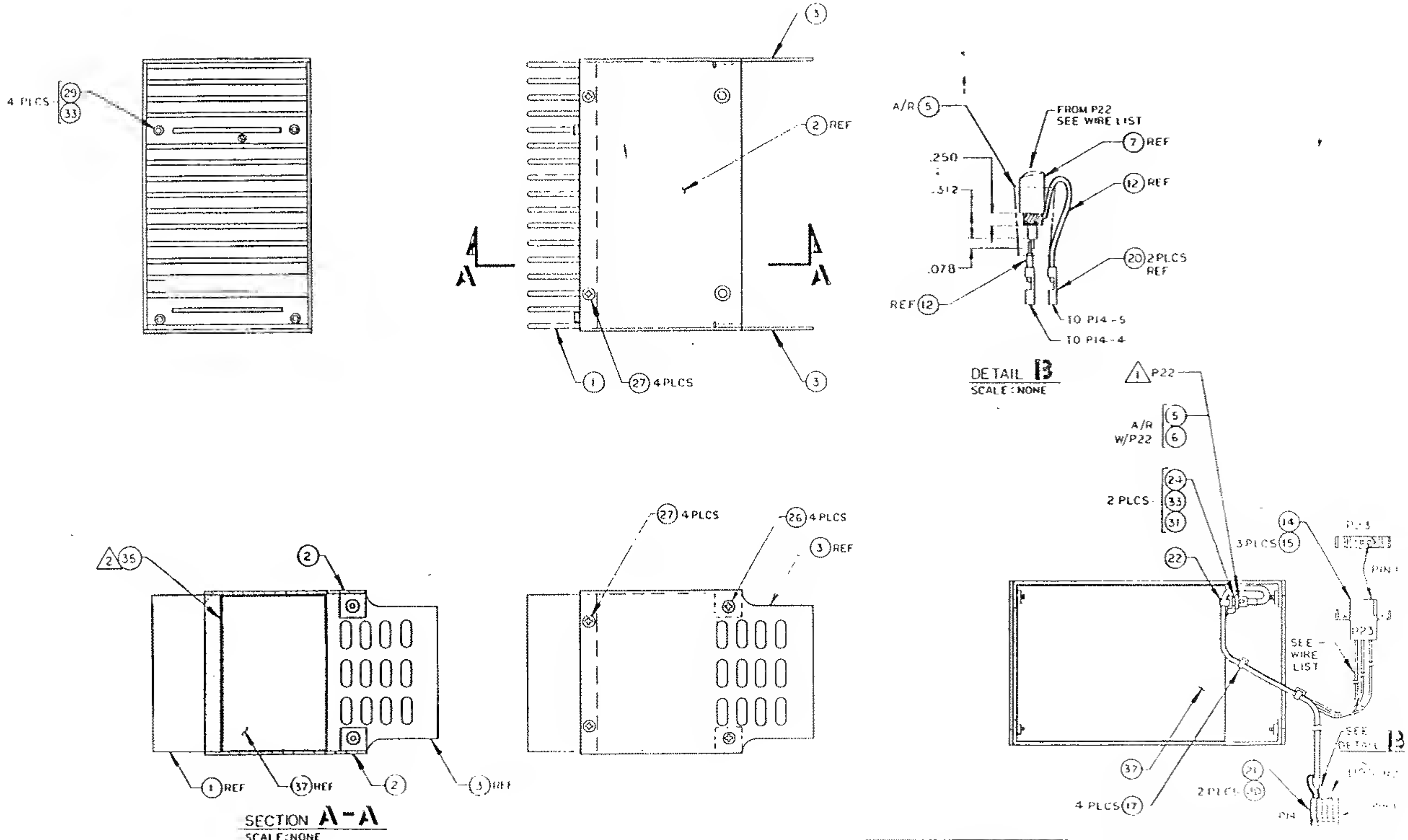
1. REMOVE OSCILLATOR PCB ASSY 401730 AND RETURN TO STOCK.

NOTES UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc.
4 GOODYEAR, IRVINE CALIFORNIA 92714

DOCUMENT TITLE			
OSC., RUBIDIUM STAND. OPTION 04R			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404469	A
SCALE 3:4		SHEET 1 OF 4	


P21/
J21
J23
P23
J14
J13
5
OPTION 04R
RUBIDIUM REFERENCE OSCILLATOR
4.2"
5.2"
P22
10 MHz BUFFERED OUTPUTS



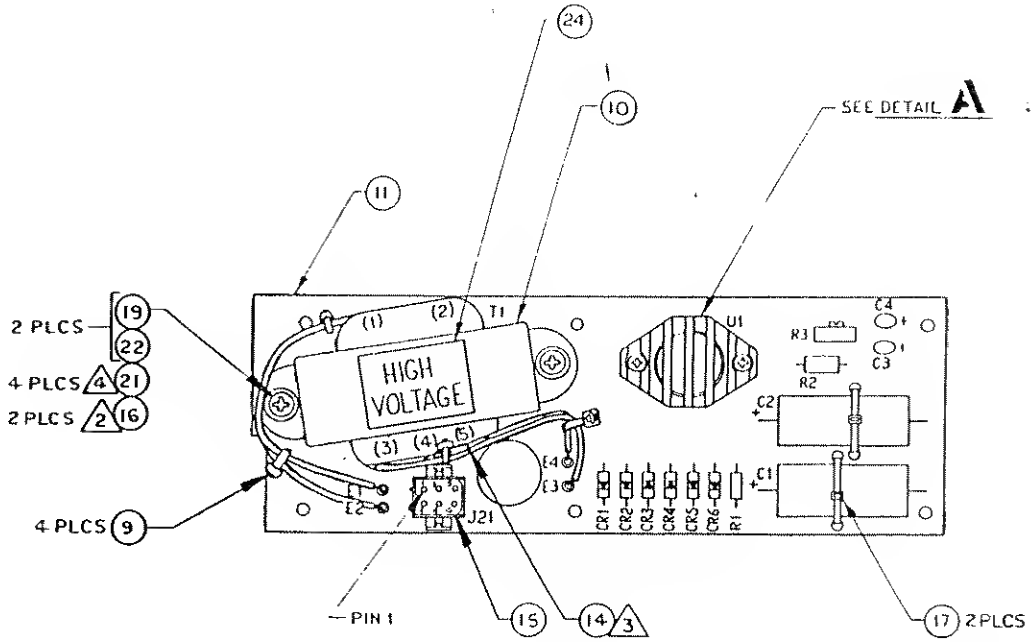
2 APPLY EVEN COATING OF THERMAL COMPOND (ITEM #35) TO BACK OF OSCILLATOR (ITEM #37) PRIOR TO MOUNTING TO HEATSINK (ITEM #1).

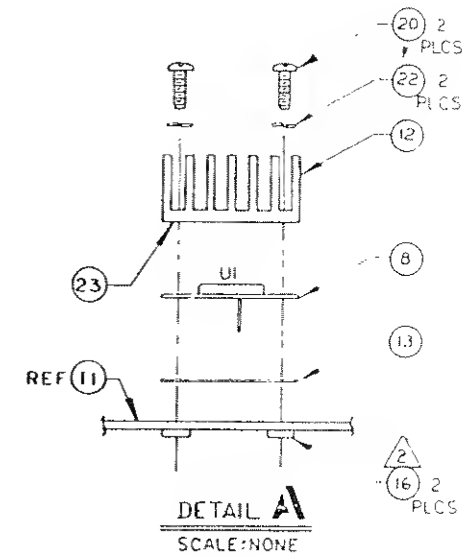
1 CONNECTOR (P22) IS SUPPLIED WITH OSCILLATOR (ITEM 37).

NOTES UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc.
4 GOODYEAR IRVINE CALIFORNIA

DOCUMENT TITLE			
MODULE ASSY, RU OSC			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
D	21793	404565	A
SCALE FULL		SHEET 1 OF 4	





DETAIL A
SCALE: NONE

4 INSTALL ITEM 21 (FLAT WASHERS) 4 PLCS, 1 EACH BETWEEN ITEM 22 (LOCKWASHER) AND ITEM 10 (TRANSFORMER) AND 1 EACH BETWEEN ITEM 10 (TRANSFORMER) AND ITEM 11 (PCB).

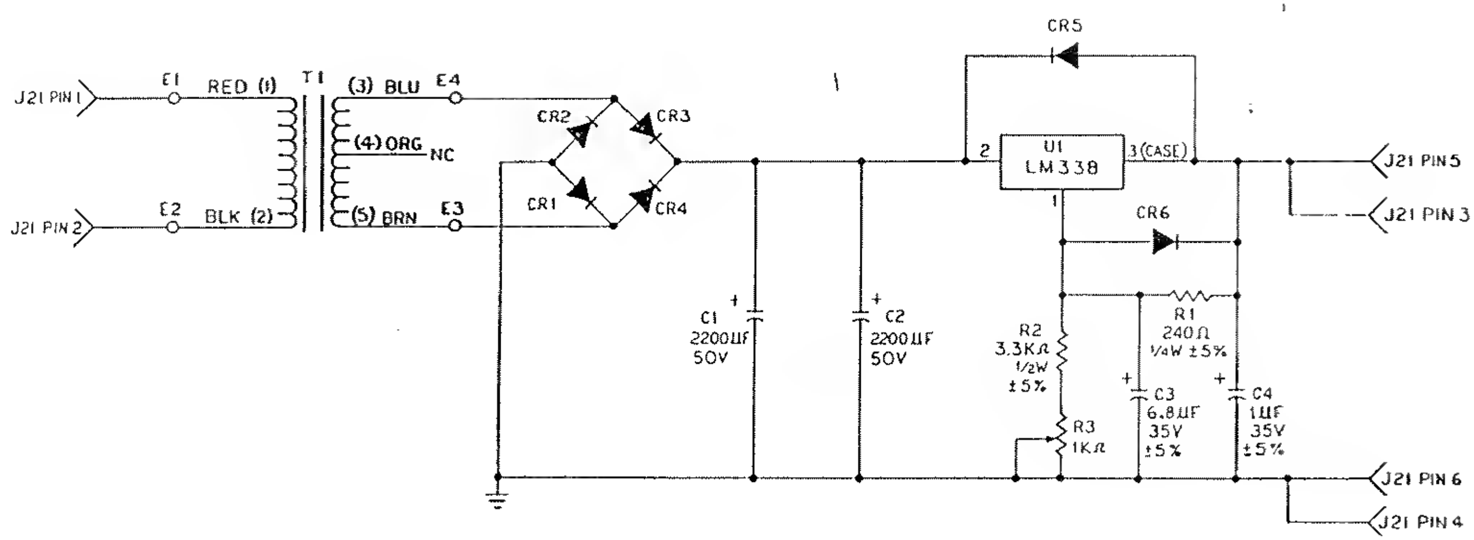
3 CUT TRANSFORMER LEAD NO. 4 TO APPROX 1 INCH LG. COVER END WITH SLEEVING, ITEM 14.

2 INSTALL PRESS NUTS ON CIRCUIT SIDE.

1. REF. SCHEMATIC 431858.

NOTES UNLESS OTHERWISE SPECIFIED

PROPRIETARY NOTICE			
RACAL-DANA Instruments Inc. 4 GOODYEAR, IRVINE CALIFORNIA 92714			
DOCUMENT TITLE PCB ASSY, RU OSC PWR SUPPLY			
SIZE C	CODE IDENT NO 21793	DOCUMENT NO 401858	REV A
SCALE FULL		SHEET 1 OF 3	



1. DIODES ARE IN4004

NOTES UNLESS OTHERWISE SPECIFIED

RACAL-DANA Instruments Inc. 4 GOODYEAR IRVINE CALIFORNIA 92714			
DOCUMENT TITLE SCHEM, RU. OSC. PWR SUPPLY			
SIZE	CODE IDENT NO	DOCUMENT NO	REV
C	21793	431858	A
SCALE		SHEET 1 OF 1	

List of Suppliers

FSC	SUPPLIER
00779	AMP, INC. HARRISBURG, PA
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OHIO
06915	RICHCO PLASTIC CO. CHICAGO, IL.
13103	THERMALLOY, INC. DALLAS, TEXAS
16956	DENNISON MFG. CO. FRAMINGTON, MA.
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, IL.
29005	STORM PRODUCTS CO. LOS ANGELES, CA.
46384	PENN ENG. & MFG. CORP DOYLESTOWN, PA.
53387	THREE (3) M CO. ST. PAUL, MINNESOTA
53894	AHAM, INC. RANCHO CALIFORNIA, CA.
55761	EFRATOM IRVINE, CA.
58730	THOMAS & BETTS CO. ELIZABETH, NJ.
70903	BELDEN CORP. CHICAGO, ILLINOIS
73138	BECKMAN INSTRUMENTS FULLERTON, CA.
78189	ILLINOIS TOOL WORKS. INC. (SHAKEPROOF DIV.) ELGIN, ILLINOIS
81349	MILITARY SPECIFICATION
8C945	ELECTRONIZED CHEMICAL CORP. BALTIMORE, MD. DIVISION OF 3M (FSC 53387)
91833	KEYSTONE ELECTRONICS CORP. NEW YORK, NY.
92194	ALPHA WIRE ELIZABETH, NEW JERSEY
95075	ENSIGN COIL CO. BURRIDGE, IL.